Chapter 5

Detector Mounting and Readout

5.1 Introduction

In this chapter, I discuss in detail the detector-mounting hardware and readout electronics. Figure 5.1 shows a tower with 4 BLIP detectors in their Run 19 positions. The detector mount and tower provide mechanical support and electrical connections to the detectors, support the cryogenic components of the front-end amplifiers, and heat-sink the wires travelling between the two.

The mounts hold the detectors and present the various detector signal and biasing lines on their outer faces. The detector package, consisting of the four detector mounts stacked together with endcaps attached, is suspended rigidly from the tower. Coaxial wire assemblies provide electrical connections from the mounts to the tower. The tower consists of four temperature stages: mixing-chamber (MC), cold plate (CP), still (ST), and LHe (4 K), corresponding to temperature stages of the Icebox. Thermal standoffs separate the stages. Wires run up the sides of the tower from the MC stage to the 4 K stage, with heat sinking at each stage. For each detector, a printed-circuit board holding JFETs is mounted at 4 K. The JFETs (referred to simply as “FETs” in the following) are the input terminals of the front-end amplifiers. These “FET cards” interface to copper-kapton striplines that connect to a room-temperature hermetic electrical feedthrough. An electronics crate is mounted near the hermetic feedthrough and houses front-end electronics boards holding detector-biasing circuits and the remainder of the front-end amplifiers.

The detector-mount, tower, and FET-card designs discussed here are the work of Dan Akerib, Bernard Sadoulet, Dennis Seitz, Tom Shutt, Garth Smith, Walter Stockwell, Roy Therrien, Storn White, and myself. The tower and FET-card thermal design was developed by Dan Akerib, Tom Shutt, and Walter Stockwell and is discussed in detail in Walter Stockwell’s dissertation [108]. Dan Akerib, Dennis Seitz, and Storn White were responsible for design and production of the striplines. I review some of this material. The detector-mount and tower designs have been changed since last documented in [108], so I discuss these new features in some detail. The front-end electronics boards were developed and have been used in the Berkeley group since BLIP detector development began in the late 1980s. Contributions have been made by a large group of people: Alan Cummings, Yannick Giraud-Heraud, Bernard Sadoulet, Dennis Seitz, Tom Shutt, Walter Stockwell, and Dominique Yvon. The 9U-format boards used in Run 19 were produced under the supervision of Mike Crisler and Steve Eichblatt at Fermilab.
Figure 5.1: Detector mount and tower. The close-packed detector mounts for 4 detectors are shown at the bottom. The endcaps of the detector assembly are not shown. The separate Q (ionization) and P (phonon) rings that make a single close-packed detector mount are indicated. The Q and P Detector Interface Boards (DIBs) are shown for one detector. The thin vertical pieces are coaxial wire assemblies (side coaxes). The four temperature stages of the tower are shown, separated by graphite-tube thermal standoffs. The tab sticking out the side of the MC stage ("MC foot") indicates the mount points to the MC lid of the Icebox. The tabs sticking out the sides of the other stages receive thermal straps from the Icebox. The tower infrared-blocker boards are indicated. A FET card is shown at the top. A stripline (not shown) connects to the top of the FET card.
5.2 Detector Mounts

The detector mounts used for BLIP detectors have evolved significantly from the original design. I present some of the history here to motivate the design of the present mounts.

5.2.1 Minimal Mass

The initial design goal for the detector mounts was to minimize the mass of material near the detectors. Any material near the detectors is a low-energy-photon source (via Compton scattering of higher-energy photons) as well as a neutron source. The original mount design is elegant, consisting of a low-mass hexagonal copper ring with support feet holding the detector at 6 points, as shown in Figure 5.2. The detector rests on sapphire balls at these points; sapphire has low thermal conductance. The sapphire balls are coated with gold on the side touching the detector to prevent the sapphire from cracking the germanium when cooled. Electrical connections are provided by wirebonds from the detector to thin copper-kapton printed-circuit boards mounted above and below the detector (called “Y”’s because of their shape).

Tests of this mounting scheme at the UCB Test Facility demonstrated that, because of the open design, infrared radiation emitted by the FETs (which self-heat to 120 K, yielding a blackbody spectrum peaked at $\approx 35 \, \mu m$) reaches the detectors at 20 mK and degrades the ionization measurement by ionizing neutralized impurities (see Chapter 4). A number of modifications were made to absorb and block infrared radiation. Primary among these is the use of a “sock,” a 0.25-mm-thick copper foil assembled around the detectors and attached to the MC stage of the tower. Residual gaps are sealed with copper tape.

The prototype Ge BLIP detector, E5, was operated at SUF in Runs 13 and 14 during summer and fall, 1996, in this type of mount. An exposure of 1.2 kg d was collected using this 60-g detector. A significant rate of veto-anticoincident low-ionization-yield events at low energy ($< 100 \, keV$) was observed: about $3 \, keV^{-1} \, kg^{-1} \, d^{-1}$ in the range 20 to 40 keV [109]. The physics of these “dead-layer” events is discussed in Chapter 4; they are caused by low-energy electrons.
CHAPTER 5. DETECTOR MOUNTING AND READOUT

incident on the detectors. The minimal-mass mount provides no protection from sources of low-energy electrons on surfaces visible to the detector.

5.2.2 \(\beta\)-Coffins

In response to the above high rate of low-yield events, the mount was modified to completely enclose the detector in a small copper box, a design which provides a number of advantages. First, it clearly delineates the surfaces that the detector sees — only the inner faces of the box. These faces can be treated to remove low-energy-electron sources. Second, the detector can be mounted in its package under full cleanroom conditions, reducing the cleanliness required when attaching the detector to the tower; it is this latter step that is performed more frequently and could lead to detector contamination. Finally, by bringing these visible surfaces closer to the detector, the design increases the likelihood that particles associated with the generation of low-energy electrons also hit the detector, moving the events out of the 0-to-100-keV region. An example would be high-energy photons that eject electrons from the copper.

This design, somewhat morbidly named the “\(\beta\)-coffin” by Storn White, is shown in Figure 5.3. Copper sheets of 1-mm thickness cover the top and bottom surfaces of the detector, with small holes to allow wirebonding. The sides of the mount are constructed from thick copper. The Y’s are glued to the outside faces of the copper sheets. “Umbrellas,” consisting of small copper sheets on standoffss, cover the holes in the mount where wirebonds enter. The sapphire ball supports were abandoned, primarily for convenience. Pyramids of kapton are attached to the copper support feet such that the pointed end makes contact to the detector. The point has a small area and thus low thermal conductance.

During Runs 15 and 16, in winter and spring, 1997, two BLIP detectors were operated in these new mounts at SUF. One of the detectors was E5, remounted but otherwise unmodified. The second detector was BLIP1, the first full-size (165-g) Ge BLIP detector. Exposures of 0.9 kg d and 2.5 kg d, respectively, were collected using these detectors. Low-ionization-yield event rates of 3 keV\(^{-1}\) kg\(^{-1}\) d\(^{-1}\) and 0.5 keV\(^{-1}\) kg\(^{-1}\) d\(^{-1}\) in the range 20 to 40 keV were observed in E5 and BLIP1, respectively [111]. That is, E5’s rate was unchanged while BLIP1 showed a rate lower by a factor of approximately 6. The large discrepancy is most easily explained by the fact that E5 was a prototype and suffered numerous cooldowns and remountings at UCB before being run at SUF, while BLIP1 was a relatively virgin detector. E5’s low-yield event rate is due to surface contamination accumulated during these numerous remountings. The E5 low-energy-electron rate is thus not indicative of achievable rates. Since no control data set is available, the source of the > 20-keV low-yield events in BLIP1 is not clear. The copper of the \(\beta\)-coffin and detector surface contamination are equally valid suspects.

5.2.3 Close Packed

Given the above results, a new mount was designed, shown in Figure 5.4, with the goal of using the detectors themselves to shield each other from external (i.e., not on the detector surfaces) low-energy-electron sources. The detectors are packed close together with no intervening material; copper endcaps close the ends of the detector stack. This design is very different from the \(\beta\)-coffin mounts, in which each detector sees copper in all directions. In this “close-packed” geometry, a large fraction of the solid angle visible to the inner electrode of a detector is occupied by another
**Figure 5.3:** $\beta$-coffin. The detector is visible at the center. In the top view, the inner circle indicates the edge of the detector flat. The pie-shaped pattern is the thermal heat sink and electrical connection to the detector ground plane. The squares above and below indicate the thermistor positions. The pads to the left of center provide contact to the resistive boron implant for applying heat pulses. The open slot to the right allows light from the LED package (above the slot) to reach the detector. The phonon-side umbrella is the large square at the center. In the side view, the walls and top and bottom faces of the detector mount are shown. The floating copper pieces are the umbrellas (top is ionization).

detector. With the inner-electrode radius being 22 mm, the expected rate reduction for inner-electrode events due to an external low-energy-electron source as a function of detector separation is shown in Figure 5.5. A 3.5-mm detector separation is used, which is the smallest spacing that can accommodate the $\approx 2.5$-mm thermistor thickness and the associated wirebonds, giving an expected reduction of a factor of 5. On the other hand, if the residual rate is due to surface contamination on the detectors themselves, no rate reduction is expected.

In addition to this “self-shielding,” the close-packed configuration allows low-energy electrons to multiply scatter. The back-scattering probability for electrons in the energy range 10 to 100 keV is about 30% [87]. While this is not large enough that vetoing multiple-scatters would yield a significant rate reduction, it is large enough to see the effect. Furthermore, multiple-scatter phenomena can be used to check an alternate hypothesis, that low-energy electrons are ejected from surrounding materials by high-energy photons rather than being emitted by a $\beta$-decaying radioisotope. The former phenomenon was first noticed by Thushara Perera and Dan Akerib in their simulations of photon-calibration data sets [132]. The two phenomena are distinguishable by comparing the ionization yields observed for multiple-scatter events in adjacent detectors; the electrons-only mechanism results in low-yield events in both detectors, while the photon/electron mechanism should result in significant fraction of high-yield/low-yield pairs.

A third design change was to cover the inside of the copper detector housing with 2-mm-thick wafers of detector-grade germanium. The wafers are etched using the same procedure as for the detectors and thus are expected to be equally clean (or dirty). In fact, since no picene wax mask is used on the wafers, they may be even cleaner than the detectors. If the electron source is surface contamination of the detectors, there should be no reduction of the low-energy-electron
rate, while electrons emitted by surface contamination of the copper should be stopped by the Ge wafers. The photon/electron mechanism mentioned above would also show no reduction with the addition of Ge shielding. It is possible to cover approximately 90% of the exposed copper of the housing with germanium wafers, whose shapes are shown in Figure 5.6. The wafers are not rigidly attached because the relative thermal contractions of copper and germanium would cause the germanium to shatter. Rather, notches are cut in the germanium wafers, as if the germanium were to be screwed down to the copper, but the screws are left loose so the wafers are free to slide and contract.

Innovations were also introduced in the mechanical aspects of the design. Previous designs were not light-tight. The copper-foil sock used to block IR radiation must be disassembled and reassembled whenever a detector package is removed and reinstalled. The sock requires copper tape to seal cracks and so is time-consuming to build. In contrast, the close-packed assembly uses infrared-blocker boards to provide electrical feedthroughs while sealing the package against light leaks, as shown in Figure 5.7. An IR blocker consists of a copper-kapton-copper circuit board with metallized penetrating holes isolated electrically from the ground plane of the board. Sockets or pins are soldered into the holes to permit electrical signals to travel through the board. Even at the break between the holes and the ground plane, the circlex substrate of the board helps block IR radiation because it is capable of (though not particularly good at) absorbing IR [108]. All wirebonds are made to Detector Interface Boards (DIBs) inside the package; these boards have Mill-Max sockets soldered to them that penetrate the blocker boards. These penetrations are made light-tight by soldering the sockets into the blocker boards.

Another problem seen with previous designs is that the copper feet supporting the detector are thin (0.5 mm) and relax over time. This allows the detector to “jiggle” in the mount, yielding mechanical impulses that disturb the detector thermal system, adding noise, producing pulses, or, in some cases, making the detectors inoperable. In the close-packed mount, the detector sits on three 1.5-mm-thick ledges, as seen in Figure 5.4; the ring and ledges are machined from the same block of copper. On the top side, the detector is pushed against two stiff copper blocks with slanted faces that make contact to the curve of the detector, also shown in Figure 5.4. At the third point of the top face, a restraint with a similar profile to the stiff supports but with two tensioned Kevlar straps is pressed against the detector, shown in Figure 5.8. The Kevlar remains tensioned while cold. Since the germanium contracts less than the surrounding copper ring, the detector is held even more tightly while cold. Electrical isolation from the copper ledges and blocks is provided by 0.13-mm-thick (5-mil) kapton at all points of contact. The larger thermal conductance resulting from the increase in contact area appears to have had no serious effects on the phonon-channel pulse height or time constants, which were discussed in Chapter 4.

A final modification is the removal of all electrical components from the detector mount. The detector biasing and signal circuits use thin-film resistors and capacitors; connections are made using wirebonds. In the earlier mounts, these components are placed on the Y’s above the detectors. Repair of damaged components requires that the whole detector mount be removed from the tower. Furthermore, the circuit boards are not protected. Given the large number (≈ 40) of components and bonds necessary, electrostatic damage to the components or accidental damage to wirebonds has occurred frequently enough to be inconvenient (two ionization coupling capacitors were shorted this way in Run 18). In the close-packed assembly, the circuit board holding all the components is moved to the basement side coax (see next section). The only electrical component
on the DIB is the LED used for detector neutralization; see Figure 5.9. The wirebonds between the detector and the DIB are completely protected once the detectors are stacked and the endcaps attached. The other electrical components lie under a protective cover on the Side Coax Assembly Board (or SCAB) at the detector end of the basement side coax; see Figure 5.10. The side coax can be assembled, all electrical components attached and wirebonded, and the whole assembly cryogenically tested independently of the detector mount.

One disadvantage of the close-packed design is that the capacitance between detectors becomes very large, leading to two cross-talk effects. First, the thermistor bias applies a $\sim 10$-mV-rms sine wave across the thermistors, only 1 mm from the adjacent detector’s ionization electrodes. There is significant cross-talk of this bias. This can be reduced by a factor of 10 by biasing the two thermistors 180 degrees out of phase, but perfect cancellation is not possible because the two thermistors possess somewhat different capacitances to the adjacent detector and different electrical characteristics. Second, a large ionization pulse in one detector produces significant cross-talk to adjacent detectors because the large inter-detector capacitance lets the detector draw current from the adjacent detector’s ground plane. The capacitance between the inner electrode of one detector and the adjacent detector’s ground plane can be estimated assuming a simple cylindrical capacitor with radius 22 mm (the inner-electrode radius) and plate separation 3.5 mm (the detector separation), giving $C = 4$ pF. The coupling capacitor to the amplifier has $C_c \approx 330$ pF, so $\sim 1\%$ cross-talk is expected. Thus, large pulses can disturb the adjacent detector. As is discussed in the next chapter, it is necessary to discard events where one detector has a large ionization pulse. Fortunately, WIMPs should interact in only one detector and produce $< 100$-keV pulses, so such a cut has no effect on the experiment’s sensitivity.
Figure 5.4: Close-packed detector mount. Top: top view, phonon side. The detector is shown in the center, phonon side up. The two circles indicate the edge of the detector and the edge of the detector flat. The circle with the indentation is the inner-outer-electrode break (etched into the contact on the ionization side). The three ledges on which the detector sits are shown (one is hidden underneath the DIB). The large squares on the detector are the thermistor positions. The “T” between them serves both as the connection to the detector ground plane and as the thermal heat sink. The two small rectangles inside the “U” make contact to a resistive patch of boron implant used for applying heat pulses. The phonon DIB is also shown. The chip-LED pair is connected to the left-most bond pad. Bottom left: side view along a midline running bottom to top. The phonon side is at the bottom. The detector separation is $\approx 3.5$ mm. Bottom right: side view along a midline running left to right. A stiff support foot is shown.
Figure 5.5: Expected inner-electrode event rate for an isotropic, external, non-penetrating radiation source as a function of close-packed detector separation. The detector parameters assumed are listed on the plot. The effect of the curved BLIP edges is taken into account. The rate is normalized to the rate in the absence of other detectors (separation $\rightarrow \infty$). The separation used for the close-packed BLIP package is 0.35 cm. Calculation by T. Shutt.
CHAPTER 5. DETECTOR MOUNTING AND READOUT

Figure 5.6: Germanium shield pieces. The lower right piece covers half of an endcap face; the other pieces cover inner faces of the detector rings (there are two ring faces that use the same type of piece). The notches accept 0-80 screws; they are slotted to allow for thermal contraction and for ease of cutting.

Figure 5.7: Face-on and side views of infrared-blocking electrical feedthroughs. The sockets feeding through the blockers are also soldered to the DIBs, as seen in the side view. The faces of the adjacent detector rings are shown to indicate how the blocker boards cover the holes in the ring walls. Unused blocker board holes are filled with solder.
SECTION 5.2. DETECTOR MOUNTS

Figure 5.8: A detector and ring with a “kevlar” foot. Kevlar straps (not shown) loop through the holes in the foot and make contact to the detector on its curve.

Figure 5.9: Detector Interface Boards (DIBs), Q (left) and P (right). The bond points are the large squares near the curved top edges. A chip LED is placed on each of the two leftmost pads. Mill-Max sockets attach to the large rectangles at the bottom edge.

Figure 5.10: Side Coax Assembly Board (SCAB). The positions of the 40 MΩ resistors are indicated by squares with two dots (R1 to R6, 24 total). The ionization coupling and feedback capacitors sit on the squares marked C1–C4. The circular points marked P2 and P3 are the positions of the Mill-Max pins that mate to the sockets on the DIBs. P1 indicates the points where the tensioned NbTi wires of the basement side coax are attached; the signal names are given. Figure taken from [133].
5.3 Tower and Cold Electronics

The detector tower serves a number of purposes. It:

- provides a removable mount for the detectors and cryogenic electronic components;
- provides low-capacitance, microphonically clean, electrical connections between the FET card and the detectors;
- provides a path for the power dissipated by the front-end FETs (approximately 7 mW per FET) to flow to the LHe bath;
- heat-sinks the aforementioned connecting wires to maintain reasonable power loads on the MC, CP, and ST refrigerator stages in spite of the large power dissipation at the 4 K stage and the natural power flow between the various temperature stages;
- and is modular: many components (detectors, basement side coaxes, FET cards) can be removed and replaced without significant disassembly. All connections are made using high-quality connectors: soldering or screw terminals are not used for connections that are frequently remade.

I discuss qualitatively the tower design. Walter Stockwell’s dissertation presents the numbers behind the design [108].

5.3.1 Tower Design

A schematic of the tower is shown in Figure 5.1. This side view shows the four temperature stages. Each temperature stage is machined from a single piece of copper and is mostly empty space. The four stages are separated by graphite tubes. The tower is hexagonal in cross section. This design permits close packing of many towers. A view of a single face is shown in Figure 5.11. Each face has 16 vertical channels in which wires are strung. Also visible are the heat-sink boards at each stage.

One purpose of the tower is to provide low-capacitance, microphonically clean, electrical connections. As discussed in Chapter 4, capacitance to ground between the detectors and the FET gates is problematic. The biggest capacitance in the readout circuit is the FET-gate capacitance of 40–60 pF, so any wiring capacitances should be small in comparison. This requirement rules out standard cryogenic coaxial cables, which have capacitances of tens of pF per foot.

Standard coaxial cables are also disallowed because they are susceptible to microphonic noise. The usual mechanism by which microphonics produces noise is discussed in Tom Shutt’s dissertation [106]. Microphonics arises from the triboelectric effect, in which a difference in the work functions of two materials in contact results in the buildup of charge at the interface [134]. The interface between the inner conductor and dielectric in a coaxial cable is susceptible to this effect. It is difficult for the surface charge on the insulator to dissipate because it is insulating. If there is microscopic relative motion of the conductor and the dielectric, some of the surface charge may be coupled directly or capacitively into conductor. Microphonics thus acts like a current source. Given the high impedances seen by the lines connecting the detector to the front-end FETs in both the BLIP ionization and phonon measurements, this current source can produce a significant voltage.
Figure 5.11: A tower face. The wire channels are visible on each stage’s face. The gaps between stages provide thermal isolation between stages; the mechanical connection is through graphite tubes (behind the face, not shown), as described in the text. The CP stage has no face (it only has feet) and so is not shown (its feet stick out through the indentations in the ST stage). The ST-stage feet are also not shown. The ST and MC heat sinks and the tower-basement side coax and tower-FET card connectors are shown. The tower IR blockers are seen edge-on.

signal. In contrast, for low-impedance devices and measurement schemes, such as a transition-edge-sensor coupled to a SQUID current amplifier, microphonics is irrelevant because the current coupled is very small.

The main driving force for microphonics in a dilution refrigerator is the flow of helium through the needle valve that feeds the 1 K pot from the LHe bath. The resulting vibrations occur at many kHz to 20 or 30 kHz. Microphonics is primarily a problem for the ionization measurement because of its large bandwidth. It can be a problem for the thermistor measurement if it extends down to 1 kHz. The obvious solution to microphonics is to remove all insulators. The tower design accomplishes this by stringing tensioned wires in metal channels. Metal covers are placed over the channels to complete the outer conductor and to protect the wires. Though these channels can be thought of as transmission lines at higher frequencies, it is not particularly useful to do so in this case; the travel time for an electromagnetic wave down the tower is less than 1 ns, much shorter than the amplifier response times, so the tower can be treated electrically as a lumped element.

The heat-sinking problem brought on by the above solution is challenging. Given the need to tension the wires, long wire runs must be mechanically supported along their entire path; i.e., one cannot simply use a long, flexible cable to provide a large thermal impedance between stages. Given the relatively short distance between the lids of the various cans in the Icebox (1 to 2 inches, typically), the available vertical height for such wire runs is small. Thus, it is necessary to repeatedly heat-sink the wires running from the 4 K to the MC stage to maintain a low power load.
on the MC stage. Heat-sink boards, consisting of 52-mil-thick cirlex (thick kapton) with copper on both sides, are used. The top side of each board is patterned with traces aligned with the wire channels. As the wires pass over the board, they are soldered down. Heat carried down the wire can flow through the cirlex to the underlying tower stage rather than flowing down the wire to lower-temperature stages. These boards are shown in Figure 5.11. An important part of the heat-sinking scheme is the use of NbTi wires, which superconduct at 9.5 K. When a superconductor is significantly below its transition temperature, a large fraction of the electrons are bound in Cooper pairs that form a Bose condensate; these pairs cannot transport heat. This greatly reduces the thermal conductivity of the wire; only phonons and broken pairs can transport heat.

Another problem brought on by the short stage separations in the Icebox is that the temperature stages of the tower are themselves separated by only 1 to 2 inches also. Graphite tubes are used to separate the stages of the tower because of their intrinsically low thermal conductance. G-10 would have been preferable, but is disallowed because of its high radioactivity. Because the thermal conductance of a tube goes like $A/h$ where $A$ is the cross-sectional area (of the graphite alone) and $h$ is the tube height, it is desirable to minimize the tube-wall thickness and maximize the height. The tubes have a wall thickness of 1.5 mm (60 mils), set by what can be reasonably machined. The height thus determines the conductance. As one can see, the tower stages have been designed to increase the tube heights beyond what is allowed by the Icebox temperature-stage separations alone. The CP stage of the tower is used only as a thermal intercept for the graphite tubes; wires are not heat-sunk at this stage.

Another issue is the thermal connection of the various temperature stages of the tower to the corresponding stages of the Icebox. As discussed in Chapter 3, the Icebox cans are not rigidly connected to one another. Therefore, the tower may be connected to the Icebox rigidly at only one layer. The MC stage of the tower is rigidly connected to the MC can lid of the Icebox at the six “feet” shown in Figure 5.1. The other temperature stages are connected to the corresponding can lids by flexible heat straps made from welding cable. The conductivity requirements on these straps are nontrivial, especially at the 4 K stage due to the large power dissipation of the FETs.

Because the wires travel down empty channels, these channels act as light leaks for the blackbody radiation emitted by the FETs. To address this problem, infrared-blocking boards are implemented at the MC and 4 K stages. The tower IR blockers are very similar to those used in the detector mounts. Blockers of this type are installed at the bottom of the FET card, where it plugs into the tower, and at the MC stage of the tower, between the heat sink that receives wires from warmer stages and the connector to the basement side coax. The MC-stage blocker abuts the MC-stage tower-mating flange, sealing the gap. At the 4 K stage of both the Icebox and the test facility refrigerators, copper-kapton-copper radiation shields that overlap the 4 K IR blockers are attached to the corresponding flanges; these shields seal the gap at 4 K without a rigid connection to the tower.

Finally, to provide convenient mate-demate connectors for the FET card at the top of the tower and the basement side coax at the bottom, Mill-Max sockets are soldered to the boards. At the 4 K stage, the sockets are laid on their sides so the socket openings point upward toward the FET card; these mate to the pins sticking through the IR blocker board attached to the bottom of the FET card. This design allows FET cards to be easily mated to or demated from a tower that is already installed by moving the cards vertically. In practice, this is important when installing a tower with many detectors. The sockets at the MC stage point horizontally outward from the
SECTION 5.3. TOWER AND COLD ELECTRONICS

233
tower itself. Pins on the basement side coax mate to these sockets.

5.3.2 Tower Construction

Assembling the tower proper is fairly trivial. Circular grooves at the points of attachment of the graphite tubes to the tower stages locate the tubes. Stycast 1266 epoxy is applied in the grooves using a syringe, the tubes placed in the grooves, and the stages stacked vertically. Alignment fixtures are used to ensure all four stages are centered and azimuthally aligned. The gap between stages is set by inserting spacers at the faces. Assembly is performed in two steps, epoxying the bottom ends of the tubes in one pass and then the top ends after the first set of epoxy joints have cured; this prevents epoxy from leaking out of the grooves and running down the tubes while upside-down.

Wiring the tower is nontrivial. There are many issues to consider. First, the wires must be selectively etched. Solder does not wet to NbTi, so the wires are clad in Cu, which is solderable. This cladding is a pure (not alloyed) normal metal, so it is a good thermal conductor. The cladding must therefore be removed on the sections of wires between heat sinks, which can only be done by etching with nitric acid. Second, the wires must be tensioned: since there is no insulator in the wire channels, the wires must be prevented from touching the channel walls. Copper shrinks more than NbTi when cooled, so the wires must be overtensioned to remain taut when cold. Third, even though low-activity solder is used [135], it is undesirable to perform soldering on the tower itself: flux may leak under the heat-sink boards, and even into the tower itself. Any solvents used to clean solder joints inevitably leak into the tower also.

To address these problems in a way amenable to mass production, Garth Smith and I developed a new wiring procedure in preparation for Run 19. It was realized that the wires themselves are strong enough to support the heat sinks. Thus, rather than solder the wires to the heat sinks on the tower, soldering is done away from the tower and the cleaned wire/heat-sink assembly transferred to the tower. A fixture was designed to place the heat-sink boards at their nominal separations. NbTi wires are tensioned and soldered to the heat-sink boards and to printed-circuit boards on a removable transfer frame that surrounds the fixture. The heat sinks are then unscrewed from the fixture and the transfer frame disconnected, leaving a transfer frame with 16 wires strung across it and with heat sinks suspended from the wires. Apiezon Wax W [129] is thinned with toluene and painted over the heat sinks to protect them during the etch step. The thinned wax has a high surface tension and sticks to the heat sinks but does not wick onto the wires between heat sinks; when dry, the wax forms a solid mask. The entire assembly is dipped in nitric acid and the copper cladding on the wires between the heat sinks is etched away. The mask is removed using xylene. The etched assembly is cleaned in alcohol and laid over a tower face. The heat sinks are screwed down. With the heat sinks in place, the wires to the transfer frame can be clipped, leaving a fully wired tower face in place. In addition to satisfying the aforementioned needs, this procedure leaves the tower unoccupied during the soldering and etching steps (which take 2 to 3 days). Multiple faces can be prepared simultaneously, or replacement faces can be prepared while a tower with a damaged face continues to be used.
5.3.3 Basement Components

As mentioned earlier, a wire assembly, named the “basement side coax,” is used to connect the detector mounts to the wires at the MC stage of the tower. A basement side coax is shown in Figure 5.12. The design is essentially the same as that of the tower side coaxes. Vertical channels are cut in a block of copper. Copper-kapton circuit boards are placed at the two ends to receive the wires. Prior to assembly, Mill-Max pins are soldered into both circuit boards; these mate to the sockets presented by the DIB/IR-blocker assemblies in the detector mount and the tower MC-stage connector. The basement side coax wiring procedure is similar to the tower wiring procedure.

As mentioned earlier, the circuit board at the detector end, the SCAB, also holds electronic components for the detector readout. These are attached and bonded after the side coax is assembled. Covers are placed over the SCAB and over the wire channels for mechanical and electrical protection. The covers are intricately machined with recesses for the components to minimize inter-trace capacitances.

A final point is that, even though the temperatures of the two ends of the basement side coax are the same, the wires are etched anyways. At the MC stage, a second stage of heat sinking is necessary to ensure the electrical lines connecting directly to the detector are cold. No heat sink is perfect, so even though the wires are heat-sunk to the MC stage of the tower, the electrons in the wire are not fully cooled. The only thermal isolation in the electrical path between the SCAB and the detector is aluminum wirebonds, which are rather short and thus do not provide a large impedance (in spite of being superconducting). Thus, if the electrons in the traces on the SCAB were slightly elevated in temperature due to power flow down the wires, they would deposit this power directly into the thermistors. The thermal impedance provided by the long (3 inches or more) run of etched NbTi wire in the basement side coax ensures that the power flow into the thermistors is negligible.

In the design used in Run 19, the basement side coaxes are machined from 0.25-inch-thick copper blocks. They are quite strong and so are used to provide structural connection between the tower and the detector package. In hindsight, this proves to be somewhat problematic because stress is placed on the basement side coax pins while attaching the detector package to the tower. This issue has been remedied in the basement design for Run 20 by the use of a separate mechanical support for the detector package.

Finally, for the Run 19 and previous towers, a hexagon of Nantes lead (old lead, whose $^{210}$Pb content has decayed away) is screwed to the bottom of the MC stage of the tower to block the hole in the inner lead shield through which the tower is inserted. It is not clear whether this is necessary; for convenience, it has been abandoned for the Run 20 tower.

5.3.4 FET Cards

A central component of the detector readout is the FETs mounted on FET cards at the 4 K stage of the tower. As discussed in Chapter 4, the FET gates are the input terminals of the ionization and voltage amplifiers. It is advantageous to mount the FETs inside the cryostat. This reduces the length of wire between the detector and the FETs and thus the capacitance at the FET gate. Also, FET noise improves as the FET is cooled because it is Johnson noise of the drain-source channel [115]. Below $\approx 100$ K, the carriers freeze out and the FET stops operating. For the FETs used, InterFET IF4500 [115], selected for their noise characteristics, the optimal operating...
Figure 5.12: A basement side coax. The circuit board at the top hold pins for connection to the tower. The bottom circuit board is the SCAB (see Figure 5.10 for a detail view). The pins mating to the DIBs are shown in the side view.
temperature is approximately 120 K [108].

**FET-Card Design**

A schematic of the FET card is shown in Figure 5.13. The card is built up from many layers of kapton and adhesive (these cards were fabricated before cirlex was available). There are three layers of copper: one at the center and one on each face. The center layer is a ground plane. A window in the board is made during fabrication and a single layer of kapton laid over the board before the top copper layer is deposited. The edges of the window are cut so the window acts as a thermal standoff. Copper pads at the center of the window provide mount points for FETs, which are soldered in place. Platinum traces are sputtered on the window to link the pads to traces on the rest of the board. The thin platinum traces and insulating window provide a large thermal impedance, allowing the FETs to self-heat to \( \sim 120 \) K in the center of the window while the board is mounted to 4 K. A heater and a temperature-sense diode are also placed on the window near the FETs; the heater is needed to preheat the window when first turning on the amplifiers (the FETs are frozen out at 4 K and do not function until preheated). The temperature-sense diode is part of a feedback loop with the heater to fix the window temperature at its optimal value, though in practice this loop has not been used.

The remainder of the front side of the card carries the gate traces from the bottom of the window to the tower-connector pins at the bottom of the card and the drain and source traces to the stripline connector. The back side of the card carries the detector-biasing, detector-pulsing, and LED traces from the stripline connector to the tower connector. Some subtleties arise regarding grounding; there are two different grounds on the FET card, a chassis ground connected directly to...
the metal of the tower, and a front-end (FE) ground connected to FE-ground traces on the stripline but isolated from chassis. The rationale for these is discussed in Section 5.4.

To protect the FETs and to mount the card to the tower, a right-angle copper gusset attaches to the front face of the FET card; see Figure 5.1. The inside of the gusset is painted with a Stycast 1266 loaded with carbon black to absorb infrared radiation emitted by the FETs; this mixture has been used by groups using cryogenic bolometers for astronomical measurements for many years [136]. Small gaps between the gusset and the card are blocked with thin strips of kapton to electrically insulate signal traces leaving the FET window from the gusset and to block IR emission.

The soldering of the FETs in place is recent innovation. For years, it had been believed that soldering these sensitive FETs damages them. Exhaustive tests by Tom Shutt and Storn White showed that there is no evidence for this hypothesis, provided the soldering is done quickly and carefully. Furthermore, solder joints are seen to be far more reliable than joints made using silver epoxy, especially with respect to $1/f$ noise usually attributed to poor electrical connections. All the FET cards used for BLIPs 3 through 6 have their FETs soldered in place; none of these 16 FETs shows anomalous noise that can be attributed to damage from soldering.

**FET-Card Microphonics**

A nonstandard type of microphonics was discovered in the FET cards, with the cause finally isolated and a fix found by Tom Shutt and Storn White. The platinum traces on the window must overlap copper pads at the end of the window to make electrical contact to the traces on the card. However, the platinum traces are thin (3 $\mu$m) and must run over a step of height 71 $\mu$m at the edge of the copper pad. This step occurs at the edge of the window, so motion of the window stresses this joint. It was shown that this movement gives rise to microphonics by modulating the resistance of the joint. This result is somewhat surprising because no gross change in the resistance is visible except under extreme stress. Small changes in the resistance, of order tens of $\mu$Ω, can result in a noise signal on the source line because of the large ($\sim$ 2 mA) DC current flowing through the FET channel. A semi-permanent fix can be made by placing a cirlex spacer underneath the window at its edge under the joint and applying solder over the joint. This results in a slight decrease in the thermal impedance but provides a rigid support for the joint. This solution was applied to the FET cards used for Run 19 and was seen to work consistently: the Run 19 FET cards are free of microphonics. The FET cards designed for ZIP-detector operation remove this issue by moving the copper pad further back over the cirlex so the joint is always supported.

**5.3.5 Striplines**

The drain and source connections to the cryogenic FETs are carried to room temperature by copper-kapton striplines. These striplines also carry detector-biasing, detector-pulsing, and LED lines down from the warm electronics. The primary design criteria for the stripline were length, thermal conduction, and resistance. The Icebox’s E-stem length is set by the size of the shield and veto and the need to provide a significant thermal impedance between the room-temperature electrical feedthrough and the LHe layer of the Icebox. This length sets the length of the striplines. The cross-sectional area and length of the traces are determined by the desired power flow from room temperature to the LHe layer. There is also a maximum resistance requirement on the
FET-source traces, ≈ 20Ω, above which the Johnson noise of the source trace dominates over the FET-gate noise.

The striplines are a natural extension of flexible-circuit technology used in printers and plotters. However, the extreme length and multiple layers push the technology. A stripline is 115 in (2.92 m) long, 1 in (2.54 cm) wide, and 18 mils (0.45 mm) thick [137]. The stripline carries 50 traces, etched out of 1/2-oz (0.0007 mils, or 0.018 mm) copper. The traces are 5 mils (0.13 mm) wide and separated by 10 mils (0.25 mm) for the bulk of their length. For the last 1 m on the warm end, seven traces for the front-end-ground and FET-source traces are widened to 35 mils (0.89 mm) to decrease their resistance. Two complete, conductive shield layers are fabricated by sputtering 1 μm copper onto kapton; they are overlaid with kapton for protection. The shield layer is very thin in order to maintain low thermal conductance. The traces meet connector patterns on each end; these connectors mate to the FET card and the room-temperature hermetic electrical feedthrough. In practice, about half of the 50 traces are assigned to front-end ground, interleaved with signal lines, to isolate the signal lines from each other and to decrease the front-end-ground resistance. Each stripline deposits a power load of about 12 mW on the LHe layer of the Icebox [104]. Finally, though they are called “striplines,” the transmission-line properties are not of interest because the bandwidth of the detector signals is small compared to the signal travel time of tens of ns (the dielectric constant may be large, as for room-temperature coaxial cables). The stripline capacitance and inductance introduce some interesting effects in the ionization-amplifier feedback circuit, but the stripline may still be treated as a lumped element.

5.4 Warm Front-End Electronics

Because of the unique detector-biasing circuitry and noise requirements, CDMS uses custom-designed front-end-electronics boards. A 9U-format, 18-slot electronics crate with a custom backplane houses the front-end boards, one for each detector. Signals come in on 50-conductor, twisted-pair “Detector I/O” cables that connect from the Icebox hermetic electrical feedthrough to a connector on the rear of the board. Power-supply voltages are available on the backplane, carried in from a separate power-supply unit situated near the crate. The amplified analog signals are output onto a 25-pin connector that mates to a 50-foot-long, twisted-pair cable that runs to the Receiver/Trigger/Filter rack (discussed in Chapter 6). Latches and registers on each board are addressed and data read or written using a standard address/data-bus configuration on the backplane. The backplane digital bus is connected to a single “Digital I/O” board in slot 19 of the rack. The front of the Digital I/O board connects via a cable to a “GPIB Interface Box” in a nearby rack. This box contains a IOTech Digital-488 GPIB-controllable I/O register board. A computer communicates via this GPIB interface with the Digital I/O board to set the state of the front-end boards.

I briefly describe the amplifier and detector-biasing circuits as well as the other functionality of these boards. The amplifier design used to read out BLIP detectors has been discussed in great detail in a paper by Dominique Yvon [138] and in Tom Shutt’s dissertation [106]. Since analysis of these circuits, made of a number of discrete components, is rather complicated and has been presented fully in these references, I do not discuss these issues here.
5.4.1 System Design Aspects

An interesting system design feature is the use of multiple power supplies and ground returns. There are three different power-supply/ground-return sets in the front-end-electronics system: front-end ground, analog ground, digital ground. Chassis ground is an additional ground system. All four grounds are tied together at the enclosure containing the front-end-electronics racks. The purpose in having multiple supplies is to prevent large, fast signals being driven on the board from disturbing the front-end amplifiers. The front-end amplifiers, are by design, extremely sensitive: the voltage amplifier is capable of sensing pulses with peak heights of less than 100 nV with signal-to-noise of better than 1. An example where multiple supplies is critical is the thermistor-bias circuit. It switches a 10-V-amplitude square wave at 1 kHz in the initial stages of generating the thermistor bias. The large currents involved can result in voltage drops across the power-supply and ground planes. If the amplifiers used the same supply, the fluctuating power-supply and ground voltages would inject noise into the amplifier circuits. This type of effect is prevented (or, at least, mitigated) by producing the large-amplitude square wave bias in a circuit connected to the analog power supplies and grounds and only shipping it to the front-end power-supply and ground system just before it goes into the stripline, after it has been filtered into a much “friendlier” sine wave. In spite of these precautions, there is still significant cross-talk of the initial 1-kHz square wave to the ionization amplifiers.

Another aspect is the use of digital control on these low-noise analog boards. While convenient for configuring the boards, care must be taken to ensure that the digital circuits do not inject noise into the analog circuits. No clock signal is used on the digital backplane; read and write strobes synchronize address/data-bus operations. Therefore, when no configuration changes are being made, there is no digital traffic on the backplane or boards. A separate digital power supply is used to prevent power-supply and ground currents from disturbing the amplifiers. The sharp edges of digital signals from the Digital I/O board are slowed before distribution on the backplane to prevent capacitive cross-talk. Data acquisition is always halted when configuration changes are made. The double-buffering of the GPIB-control commands through the GPIB Interface Box and Digital I/O board isolates the front-end boards from the GPIB. A fiber-optic GPIB extender connects the GPIB Interface Box to the data-acquisition computers, electrically isolating the front-end digital control.

5.4.2 Front-End Amplifiers

I discuss here the basic operating principles and noise response of the front-end voltage and ionization amplifiers. Detailed discussion of how these noises affect the respective measurements has been presented in Chapter 4.

The voltage amplifier is source-follower configuration which acts, in practice, as a non-inverting op-amp configuration; see Figure 5.14. The FET gate corresponds to the noninverting op-amp terminal, the source to the inverting terminal, and the amplifier output to the op-amp output. The feedback resistors in the simplified schematic perform their same function in the real amplifier. The action of a FET is to change the channel conductance in response to a change in $V_{GS} = V_G - V_S$, where $V_G$ is the gate voltage and $V_S$ is the source voltage [139]. The amplifier senses this conductance change as a change in the drain current; it amplifies this change and applies the amplified current to the feedback-resistor network shown in Figure 5.14. This changes the source
voltage in the direction needed to make \( V_S \) track \( V_G \), thereby returning \( V_{GS} \) to its quiescent value. Hence the name “source-follower.” The amplification factor is \( G = (R_s + R_f)/R_s \approx 50 \). A second stage of amplification is provided by a standard inverting amplifier with \( G = 10 \). The main noise sources are the gate noise (the channel Johnson noise referred to the gate) and any noise on the source — Johnson noise of the source resistor, variations in the source resistance, etc. Noises at the gate and source can be modeled as noise sources at the noninverting and inverting inputs of the noninverting op-amp configuration.

The ionization amplifier is similar to an op-amp integrator; see Figure 5.15. The gate now corresponds to the inverting input of the op-amp. The amplifier output corresponds to the op-amp output. The source corresponds to the noninverting input and is grounded. Thus, gate-voltage changes cannot be nulled by moving the source. Instead, the amplifier provides current to the detector to prevent the gate from moving from ground. Viewed another way, an event puts charge on the detector (and FET-gate) capacitance, causing the gate voltage to move away from ground. This charge must be removed from the detector to keep the gate at ground. The amplifier senses the change in FET drain current when the gate moves away from ground; the output of the amplifier swings as is necessary to counter the movement of the gate. For a \( \delta \)-function current pulse containing total charge \( Q \), the voltage at the output of the circuit is \( V = Q/C_f \). The feedback resistor \( R_f \) shorts the capacitor on long timescales, producing a decaying output pulse with time constant \( R_f C_f \). A second stage amplifies this voltage pulse by a factor of 200. Noise analysis can
be done with the op-amp integrator model of the circuit and has been discussed in Chapter 4.

One interesting feature realized recently is that the speed and stability of the ionization-amplifier circuit is limited by the output impedance of the amplifier. The present configuration has an output impedance of approximately 5 kΩ. This forms a $RC$ with the stripline capacitance (∼ 100 – 200 pF). If the amplifier is sped up by modifying its intrinsic response time, the system oscillates. It is believed that this is because of the phase shift due to the $RC$. Merle Haldeman and Sae Woo Nam have implemented a version of the amplifier with a lower output impedance and have observed that the new configuration can be sped up by a factor of a few without oscillating.

### 5.4.3 Detector Biasing

The primary elements of detector biasing have been discussed in Chapter 4. I discuss here how the voltage sources for the thermistor and ionization bias are implemented.

The ionization bias is straightforward. A computer-controlled DAC provides a reference value for the voltage. This voltage is buffered to switch it over to front-end ground; it is then filtered with a passive $RC$ filter and an active op-amp integrator. As is discussed in Chapter 4, the ionization voltage bias is irrelevant on pulse timescales: the detector itself provides the bias. The purpose of the ionization bias is to recharge the detector capacitance between events. Thus, the filtering can be quite aggressive to ensure no noise is added by the bias; the $RC$ time of the filter and the integrator is 100 ms.

The phonon bias is more complex. A clean sine wave is generated on the board as follows. A DAC is set to specify the voltage of the sine wave, up to a fixed numerical factor. The DAC output is sent to the analog input of an AD630 modulator/demodulator IC, which operates, essentially, by switching an inverter in and out of the signal path based on the zero crossings of its control input. A low-amplitude 1-kHz sine wave from the backplane provides these zero crossings. The DC output of the DAC is thus converted to a 1-kHz square wave. The square wave is filtered using a 4-pole low-pass Butterworth filter with a 3 dB point of 1 kHz to produce a 1-kHz sine wave. The sine wave is buffered and switched to the front-end ground circuit. Just before sending it to the stripline, the bias is divided using a passive resistive divider. The bias is kept large while on the board to make sure that the output noise of all the components in the production path remains small compared to the bias; the bias and noise are divided by the same factor by the passive output divider, maintaining the high signal-to-noise ratio. This voltage is applied to the top of a divider network consisting of a cold 40 MΩ resistor and the thermistor, producing a current bias for the thermistor. The biases for the two thermistors on a given detector are operated 180 degrees out of phase; the resulting cancellation reduces by a factor of 10 the cross-talk to the ionization circuits on the board, on the detector, and to adjacent detectors.

### 5.4.4 Phonon Lockin

The lockin method used for measurement of thermistor pulses was described in Chapter 4. The details of the implementation are as follows. The signal output by the voltage amplifier is still in modulated form. This signal is filtered using a 2-pole low-pass filter with a cutoff frequency of 1.85 kHz to remove the third and higher harmonics of 1 kHz. The resulting signal is demodulated by an AD630 modulator/demodulator IC, switching on the zero crossings of the signal itself. The DC component of this rectified signal is determined by an integrator circuit (with 66-s time constant).
and subtracted from the rectified signal. This provides a “DC-ref” signal that is proportional to the rms value of the modulated signal; in the limit that \( RC \) rolloff at the thermistor is unimportant, this is proportional to the thermistor resistance. The now AC-coupled signal is filtered by a 8-pole low-pass Butterworth filter with a cutoff frequency of 450 Hz. As discussed earlier, this filters out the components of the signal that are shifted to 2 kHz, 4 kHz, etc. by the simple demodulation scheme. The resulting 450-Hz bandwidth is sufficient to faithfully reproduce the phonon-pulse shape for interactions in the crystal; however, thermistor events are bandwidth-limited. The output of the Butterworth filter is the pulse that is digitized.

Because the DC-level of the output of the demodulator is set by the carrier amplitude, small variations in the carrier amplitude appear as baseline drifts. The DC ref is subtracted from the demodulator output with a 66-s time constant, so long-timescale drifts are taken out and the baseline remains constant. Short timescale drifts are not corrected. If the detector temperature is very unstable for some reason, the signal baseline may wander. Events for which the signal baseline is outside a reasonable range are discarded, as is discussed in Chapter 7.

### 5.4.5 IBAPACAP

The IBAPACAP, or Implant Biasing And Pulsing and ChArge Pulsing, circuits produce pulses to mimic events. As mentioned in Chapter 4, a small resistive heater (\( \sim 100\Omega \)) on the detector can be used for DC heating or to produce heat pulses. Pulser capacitors are placed at the gates of the ionization-amplifier FETs; step-function voltage pulses into these capacitors present \( \delta \)-function current pulses to the ionization amplifiers. Both pulser circuits are initialized and enabled via the digital interface. It is undesirable to use this interface to trigger the IBAPACAP because the digital traffic would likely cross-talk to the analog circuits and could even cause heating in the detectors. Instead, a trigger signal sent out on the GPIB is transmitted from the GPIB Interface Box on a separate, twisted-pair cable and received differentially by an auxiliary board in the electronics crate, where it is converted to a square analog pulse with slow edges and transmitted onto the backplane. Once received on each board, it is reconditioned using a Schmitt trigger. The reason for the slow backplane pulse is that, with 18 boards receiving the signal, the large line capacitance would require high-speed currents to be driven, likely resulting in cross-talk. Once the signal is received on each board, it is possible to speed up the edges again because the trace lengths and capacitances on the boards are small.

The phonon pulser operates as follows. The pulser consists of a small patch of resistive material on the surface of the detector, electrically isolated from the ionization electrodes and thermistors. A DAC sets the amplitude of the pulses to be applied to the heater pads. A one-shot sets the length of the pulse to be 50 \( \mu \text{s} \). The pulse must be short compared to the rise time of the phonon pulse to accurately simulate a \( \delta \)-function energy deposition. The sharp edges of the one-shot pulse are filtered using a 4-pole low-pass filter with a cutoff frequency of 100 kHz to prevent capacitive cross-talk to the phonon and ionization circuits. The filtered pulse is sent differentially down the pulser lines after a final passive resistive-divider stage: pulses of the same size but opposite sign are applied to opposite ends of the pulser pad on the detector to minimize cross-talk to other lines.

The phonon pulser produces pulses of a fixed amplitude at known times. At the start of a run, this is useful for optimizing the phonon bias value. The optimal bias is a complex function of refrigerator temperature, sensor characteristics, and the other sensor’s bias, and so is difficult
to calculate from first principles. The phonon pulser is used to map out the phonon pulse height versus bias empirically. During normal data-acquisition, pulser runs at intervals of a few hours calibrate the relationship between the thermistor DC ref and pulse height, allowing corrections for small drifts in refrigerator temperature.

The phonon-pulser circuit was designed with greater goals in mind. Since the voltage of the pulse and the heater-pad resistance are nominally known, it is possible to calculate the energy deposited and thus use the phonon pulser as an absolute energy calibration at low energies rather than relying on 511-keV positron-annihilation photons (see Chapter 6). The phonon pulser fails in this respect — the phonon pulser energies do not give the expected event energies. The pulse applied to the heater is not square and is probably partially shunted by parasitic capacitances in the lines down to the detector, so the incorrect calibration may not be surprising. Another goal had been to use the phonon-pulser pulses to calibrate and calculate the efficiency of the phonon-pulse-fit-χ² cut. Unfortunately, it appears that, above 50-keV phonon pulse height, phonon-pulser events deviate from the shape of events due to particle interactions. It had also been expected that phonon-pulser data could be used to measure the phonon-trigger efficiency. This turns out to be unnecessary because it can be measured using low-energy events that are acquired when another detector triggers.

The ionization pulser also has problems. For the same reasons given above, it is not used to determine trigger thresholds. It is not useful for calibrating drifts in the ionization amplifiers because the pulser itself is as susceptible to drifts as the ionization amplifiers. The ionization pulser can be used to check the resolution in ionization as a function of energy.

It is likely that these problems with the IBAPACAP could have been corrected with more work, but these issues were a low priority at the time. While the phonon pulsing scheme is not expected to be applicable to ZIP detectors, ionization pulsing may prove useful if the pulse calibration can be stabilized.

### 5.4.6 Output Stage

The output stage of the boards contain assorted conveniences. The ionization-signal polarities may be switched, which is necessary if the ionization-bias polarity is switched. Two multiplexers make various housekeeping signals available to the DAQ system: the inputs to the lockins (i.e., before demodulation), the phonon biases, the ionization biases, etc. Every signal is buffered before making it available to the outside world. Front-panel test points are buffered with OPA627’s with 50 Ω output resistors to ensure they can drive coaxial cables to oscilloscopes. Signals are output onto the 50-foot-long, 25-conductor cables that run to the Receiver/Trigger/Filter rack using LM6321 line drivers, which are capable of driving the highly capacitive loads presented by the cables while maintaining sufficient bandwidth.