Available online at www.sciencedirect.com
ScienceDirect
Nuclear Instruments and Methods in Physics Research A 591 (2008) 476–489
NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A
www.elsevier.com/locate/nima

Design and performance of a modular low-radioactivity readout system for cryogenic detectors in the CDMS experiment

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Received 13 February 2008; received in revised form 7 March 2008; accepted 17 March 2008
Available online 29 March 2008

Abstract

The Cryogenic Dark Matter Search (CDMS) experiment employs ultra-cold solid-state detectors to search for rare events resulting from WIMP-nucleus scattering. An innovative detector packaging and readout system has been developed to meet the unusual combination of requirements for: low temperature, low radioactivity, low energy threshold, and large channel count. Features include use of materials with low radioactivity such as multi-layer KAPTON laminates for circuit boards; immunity to microphonic noise via a vacuum coaxial wiring design, manufacturability, and modularity.

The detector readout design had to accommodate various electronic components which have to be operated in close proximity to the detector as well maintaining separate individual temperatures (ranging from 600 mK to 150 K) in order to achieve optimal noise performance. The paper will describe the general electrical, thermal, and mechanical designs of the CDMS readout system, as well as presenting the theoretical and measured performance of the detector readout channels.

PACS: 95.35.+d; 12.60.Jv; 07.20.Mc; 95.55.Vj

Keywords: Dark matter; WIMP; Cryogenic detector; TES; Phonon; Ionization; CDMS

1. Introduction

The Cryogenic Dark Matter Search (CDMS) collaboration is conducting experiments to search for weakly interacting massive particles (WIMPs) in the galactic halo using terrestrial detectors [1–5]. WIMPs are one of the favored candidates for stable relic particles produced in the early universe that would have decoupled from the hot baryonic plasma and make up the dark matter in galaxies and clusters of galaxies. The direct detection of WIMPs through elastic scattering from nuclei is challenging

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doi:10.1016/j.nima.2008.03.103

because: (i) the event rate is less than one event per kilogram of detector per day; (ii) the energy of the recoiling nucleus is typically 10–100 keV; and (iii) the background rate from residual radioactive contamination and cosmogenic activation is high. The approach taken by CDMS is to simultaneously measure, in a cooled germanium or silicon crystal, the full recoil energy using a thermal or phonon-mediated calorimetric signal as well as a more conventional ionization signal. Comparison of these measurements allows us to discriminate between electron recoils resulting from the dominant radioactive backgrounds (gammas and betas) and nuclear recoils resulting from WIMPs and neutrons, because the latter are less ionizing by a factor of ~3. (Methods for suppressing the neutron background are discussed elsewhere [5,6].)

Because of the unusual combination of requirements in CDMS—low noise, low background, high channel count, and low temperature—we have had to advance new designs and employ new materials in our detector packaging. Fig. 1 depicts the CDMS setup. The anchor for the system is a multi-temperature-stage modular coaxial wiring package, or "Tower." The nominal temperatures of the Tower stages are determined by the corresponding cooling element of the refrigerator and are: 10, 50, 600 mK and 4 K. Six detector holders with modular coaxial wiring assemblies, or "side coaxes" are mounted in the lower portion of the Tower. Cold electronics cards that carry either four FETs or two FETs and four DC Superconducting Quantum Interference Devices (SQUIDs), depending on the type of detector deployed, are mounted on top of the Tower. The electrical connections from the cards to the room-temperature vacuum bulkhead are made through a long shielded-copper flex circuit, or "stripline". Except for the warm end of the stripline, which is outside the radioactive shielding, all of the components of the Towers, stripline, electronics cards and detector packages are made from materials that have been pre-screened for U/Th isotopes. Our goal was to have <0.1 ppb U/Th content (by mass) in the material surrounding the detector package; this limit corresponds to radioactivity levels of roughly $<1\,\mu$Bq/g. The electronics sequence progresses from the detector to the side-coax, Tower face, electronics card, stripline, vacuum bulkhead connector and external "warm" electronics front-end board. In Section 2, we describe the cold hardware components in detail, including the differences between CDMS I and CDMS II, which use different types of detectors.

Both CDMS I and CDMS II use the same readout system for the ionization signal. The ionization signal is read out using amorphous silicon electrodes and FETs and is described in more detail in Section 3. CDMS I primarily used detectors in which the (thermal) phonon signal was

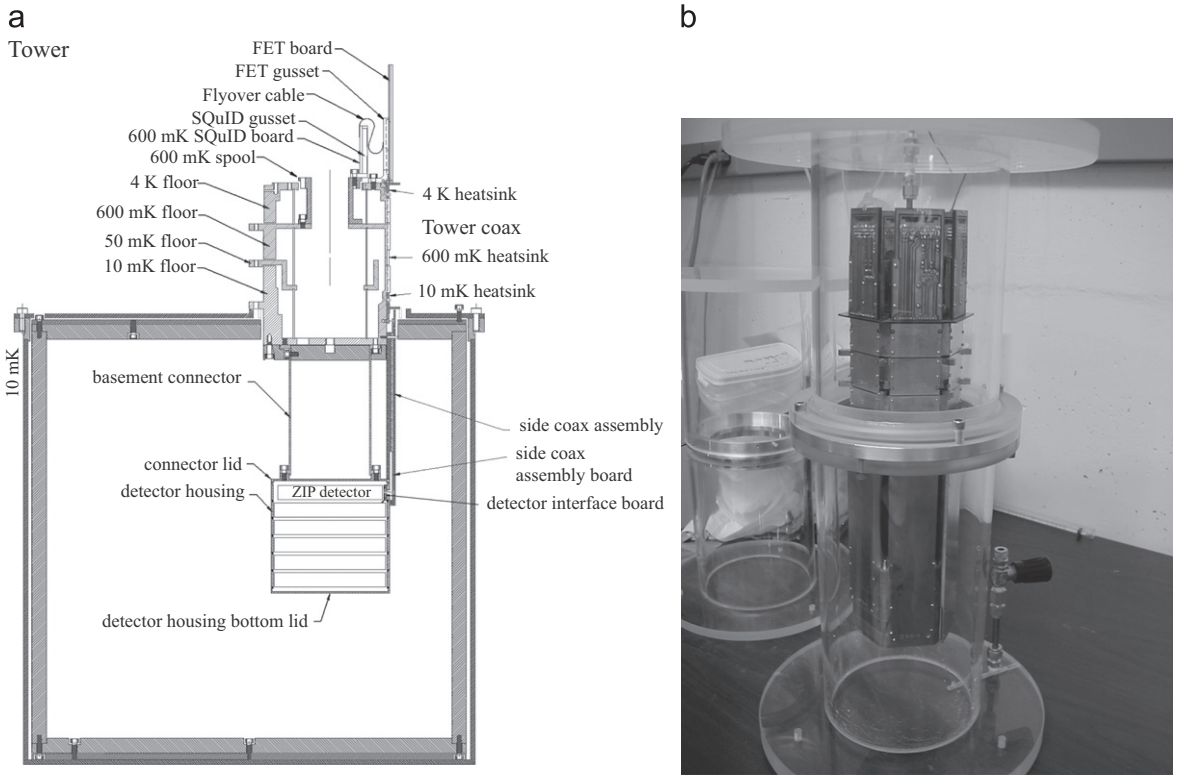

Fig. 1. Cross-section of the innermost region of the CDMS experimental setup. The outermost shown box is a cutaway view of the 10 mK can cooled by the dilution refrigerator's mixing chamber. Mounted in its lid is the cryogenic detector and wiring package, or "Tower" module. The Tower section above the lid consists of cold electronics cards and wire heat sinking. The wiring is mounted on heat sinks on the 10, 50, 600 mK and 4 K layers shown in the "Tower coax" cutaway section. The mechanical superstructure of the upper section consists of four "floors" mechanically joined but thermally isolated by thin-wall graphite tubes. The section of the Tower below the lid contains modular detector packages, each connected to one of six Tower faces by a "side coax" wire assembly. See main text for further details.

read out using neutron-transmutation-doped (NTD) germanium thermistors. These detector are discussed in Section 4. CDMS II uses detectors which rely on a similar amorphous silicon ionization electrodes as the CDMS I detectors, but use athermal phonon sensors read out by Quasiparticle-trap-assisted Electrothermal-feedback (ETF) Transition-edge sensors (TESs) (QETs) and SQUID amplifiers. This is the subject of Section 5.

2. Description of the hardware

2.1. System requirements

The specifications of the detector packaging and readout system are dictated by the low-background nature of the experiment and the requirement that the detectors be operated at a temperature below 20 mK. A detailed description of the CDMS detectors can be found in Refs. [7–13], and a description of the cryogenic systems and packaging in Refs. [5,14,15]. The detectors consist of individual short cylindrical 160 or 250 g germanium and 100 g silicon targets.

Briefly, the ionization measurement is accomplished with amorphous silicon electrodes on either side of the cylinder faces and read out through a low-noise JFET input charge amplifier [12]. BLIPs (Berkeley Large Ionization and Phonons detectors) employed a thermal measurement which was made with two NTD germanium thermistors that were bonded to the undoped germanium target and read out through a low-noise JFET input voltage amplifier. ZIPs (Z-dependent Ionization and Phonon detectors) use the same ionization readout, but employ a faster athermal phonon measurement. Phonons are sensed by a superconducting TES operated in ETF mode. Phonons are collected over a large fraction of the surface by coupling the TESs with aluminum quasiparticle traps. The signal current in the QET sensors is read out with a SQUID amplifier.

To achieve low-noise performance for both phonon and ionization signals, the first stages of amplification have to be located within the dilution refrigerator, as close as practical to the detectors. Extensive studies indicated that an essential feature of the ionization measurement FET wiring is a "vacuum coaxial" design. Microphonic pickup is greatly reduced if the central conductor is suspended in a shielded channel, free of dielectric material. This is particularly important for connections to the high impedance gate of the FET. Since each FET dissipates several mW, their heat load can only be tolerated on the 4 K stage. The FETs are coupled to the 4 K stage via a thermal standoff, which allows them to self-heat to 150 K, where FET noise is at a minimum. The 24–30 cm of wiring between the 150 K FETs and 10 mK detectors must be thermally anchored at each intervening temperature stage. The path of the connection from the FET source terminal to room temperature electronics must be kept at a low impedance compared with the transconductance of the FET, while at the same time minimizing thermal loading. Signals are brought to room temperature through the stripline, a custom designed 3 m long flex cable. Finally, since the detector package design was meant to accommodate a full system of 42 detectors with 16 wires per detector, modularity and manufacturability were important considerations.

In addition to the electrical and cryogenic constraints outlined above, the requirement of low background limited the design to the use of radiopure materials. In particular, fiberglass circuit boards and stainless steel structural elements—ubiquitous in cryogenic systems—could not be used. All circuit boards are composed of multi-layer laminates of 0.127 mm-thick acrylic based polyimid film (referred to by the product name KAPTON [16]). Thermal isolation between the stages of the Tower is achieved with thin-walled high-purity carbon tubes. All solder connections were made with custom-made low-activity solder [17]. The detector holders are light-tight copper boxes that allow the detectors within a stack to be mounted close together while shielding against events from radioactive contaminants along surface with a line-of-sight to the detectors. Minimizing material between detectors results in an increase in the probability of background photons and electrons scattering in multiple detectors, thus reducing that component of background.

2.2. Towers

The primary mechanical frame and thermal anchor for the detector package is the upper Tower. It consists of four copper sections joined by three thin-walled graphite tubes, and is shown in Fig. 1. FET cards are mounted on the top stage (one on each hexagonal face) and up to six detectors are mounted in the base. Superconducting wires mounted on the faces carry the signals from the FET cards to the base. Each copper section is thermally coupled to an element of the dilution refrigerator at nominal temperatures 10 mK (mixing chamber), 50 mK (cold plate), 600 mK (still), and 4 K (LHe bath). The wires are heat sunk by soldering to copper pads on printed circuit boards (PCB) at the 10, 600 mK and 4 K layers. The lower thermal conductivity of the superconducting wires compared with the graphite tubes allows the wires to bypass the 50 mK heat sinking. The Towers are modular and are fully wired and assembled with detectors prior to installation. They are then installed as a unit into either a test refrigerator or the shielded cryostat of the actual experiment. The primary heat load between the layers is due to the graphite tubes and is ≈ 140 nW for the 4 K to 600 mK connection: this is sufficiently low to meet the specifications of the dilution refrigerator system [14].

A key aspect of the Tower is its provision for a good signal path for the gate wire of the FETs. Extensive prototyping of early detector designs indicated that the gate wire is highly susceptible to microphonic pickup, which occurs when it is exposed to insulator surfaces that

acquire static charge, such as in a conventional coaxial cable with dielectric insulator or in a connector pin soldered into a non-plated hole in a PCB. We achieved a dielectric-free "vacuum coaxial" configuration by soldering each wire to PCBs that suspend it in machined copper channels in the upper Tower faces. A thin copper cover completes the outer conductor and with the copper channels provides a shielded low-capacitance path. The solder pads on the PCBs also serve to heat sink the wire to the associated layer of the refrigerator. Although immunity to microphonics is only required for the gate wires, we suspend all other readout wires in the same manner. Although the PCB solution lends itself to an efficient production mode, the steps of construction are still quite involved. In particular, only a low-activity solder with minimal flux may be used [17]. Superconducting wires are used since they result in a low electrical impedance and low thermal conductance path. Copper or nickel cladding is required in order to solder the superconducting wires; however, fully clad wires would present a significant thermal heat load. We selectively etch the cladding to establish a thermal gradient between the heatsinks. We use 0.066 mm diameter copper cladded NbTi wires (with 0.0406 mm core diameter). After soldering the wires to heatsink boards on a transfer frame, a wax mask is brushed on to protect all surfaces except for the unwanted copper, which is then etched with nitric acid. After the wax is removed, the wires and PCBs are transferred to a Tower face.

Additional considerations arose while testing and this design. Since conventional fiberglass circuit boards are disallowed due to high potassium contamination (in particular, the long-lived beta emitter ^{40}K), the circuit boards were originally made from KAPTON. More recent versions of the Tower use board made from CIRLEX (1.5 mm-thick polyimid film with no acrylic content, also manufactured by DuPont). Also, conventional connectors with black thermoplastic housing typically had high radioactive contamination. Care was given to choosing a connector, leading to a suitable candidate, an all metal connector pin/socket combination (manufactured by MILLMAX Corporation), which is used for all cryogenic connections throughout the experimental setup. The contact resistance for these connectors is $\sim$2 mΩ and their non-trivial impact on the low impedance SQUID circuits will be discussed further in Section 5. Further details of the detector packaging can be found in Ref. [15].

The CDMS I results presented in Refs. [5,6] were obtained using a stack of four BLIP detectors operated in 1999 and a single prototype ZIP detector operated in 1998. Subsequent CDMS II results were obtained using one [3,4] and two [1,2] Towers of six ZIPs each.

2.3. BLIP detector holder

The design for the BLIP detector holders was revised several times as it was being optimized. Initially we were most concerned about muon-induced neutrons in the material close to the detector; therefore, minimizing the mass of the holder was an important consideration. However, early results from the Stanford Underground Facility indicated that over 99.95% of such events can be vetoed with an outer scintillator [18], exceeding the original design goal. It also became clear that local photon and electron backgrounds from surfaces with a line-of-sight to the detectors, as well as potential surface contamination on the detectors themselves, was the dominant source of background events. This led to an approach where the detectors were mounted in a close-packed geometry with a minimum of material between the detectors.

The philosophy behind the final BLIP detector holder design was to minimize the solid angle for external sources of radiation reaching the inner electrodes of the detectors and to maximize the probability that surface contamination on the detectors themselves will produce coincident events between nearest neighbors. Additional features include placing the passive electrical components outside the small detector cavities and lining the inside of the cavities with detector-grade germanium. Using germanium, which is one of the least contaminated materials available, significantly reduced the rate from backgrounds on the surfaces surrounding the detectors.

Each BLIP detector is held in an interlocking copper ring-shaped housing and held in place on three short ledges that extend in radially from the ring. Electrical and thermal insulation is accomplished with CIRLEX standoffs between the copper housing and detector. It is necessary to hold the BLIP germanium quite firmly in order to avoid mechanical impulses which appear as thermal energy in the detectors. Electrical connections to the detector are made with aluminum wire wedge-bonded wire to a KAPTON circuit board on the side of the ring. A "side coax" connector with a geometry similar to the Tower wires connects to pins on the outside of the circuit board. Pins at two vertical levels allow connections to upper and lower surfaces of the detector. Except for an LED in the detector cavity, which is used to neutralize impurities in the detectors [19], all of the cryogenic components of the readout circuits which need to be in close proximity to the detectors are on a circuit board mounted on the side coax as shown in Fig. 3.

Up to six detector modules are assembled in an interlocking stack so as to form a closed copper cavity containing the detectors. Side coaxes of six different lengths couple each detector to a face of the Tower. Germanium-lined copper covers at top and bottom are used to seal the stack, and a spool-shaped copper tube connects the uppermost detector mount to the underside of the Tower.

2.4. ZIP detector holder

The philosophy behind the ZIP detector holder design is similar to that of the BLIP design. Similar copper housings

are used except that the ZIP detectors are of larger diameter requiring a somewhat different connection scheme. The side-coax connects to a detector interface board (DIB), which is mounted on the detector holder. The main purpose of this board is to transmit the signals from the side-coax through a MILLMAX connector and connect them (via solder coated copper traces) to the aluminum pads, from which wire-bond connections can be made to the surface of the detector. The DIB is made of 1.30 mm-thick CIRLEX with 0.036 mm thick (1-ounce) copper traces on each side. Due to the limited space, the aluminum pads were placed on the horizontal edge of the board, which was technically challenging since the tinned copper traces had to extend around the edge. This feature was accomplished by creating a row of copper plated holes in the circuit board and cutting away material to expose the plated holes on the board edge. The resulting semicylindrical troughs were then sputtered with aluminum and used for wire-bond connections to the detector surface.

In addition, the DIB holds two LEDs which are used for detector neutralization [19]. The detector itself is held in place by six 1.52 mm-thick CIRLEX pads screwed onto the holder (three on each side). The grip is made tight at room temperature and it strengthens as the detector is cooled due the differential thermal contraction of the holder's components.

As in the case of BLIP design, up to six detectors can be assembled into a stack forming a copper cavity containing detectors with 2 mm spacing between them.

2.5. Cold electronics

In the following two sections we describe the cold electronics cards that contain the FETs for the ionization and NTD-thermal measurement and the SQUIDs for the athermal phonon measurement. The BLIP detectors use four FET-based amplifiers with the FETs on a single card at the 4 K stage. The ZIP detectors also have FET amplifiers on a 4 K card to measure the ionization signal: however, the SQUIDs for the QET readout are mounted at a lower temperature on the 600 mK stage for better noise performance. In this case, the FET card has only two FETs. In the following two subsections we describe the FET and SQUID cards in detail. Fig. 2 shows a photograph of the cold electronics card as well essential portions of the connection circuitry, while Fig. 3 shows the temperature stages at which the various connections of the FET and SQUID readout circuits are made. The SQuET card is the name of the hybrid electronics card composed of the FET card (larger card, on the back left side of the Fig. 2 image) and SQUID card (smaller card, on the right), connected by the flyover. The two cards are thermally anchored to the 4 K and 600 mK layers of the Tower, respectively. The KAPTON window is under the copper gusset on the FET card (right). This drawing of the CDMS II version of the FET card describes the geometrical relationships between the KAPTON window and the stripline, flyover, and Tower connectors. It also shows the design of the KAPTON window. The CDMS I version of the FET card does not have the flyover connector and its KAPTON window extends to the full width of the card, hosting four (instead of two) FETs. The card measures approximately 3.8 cm wide ×9 cm tall.

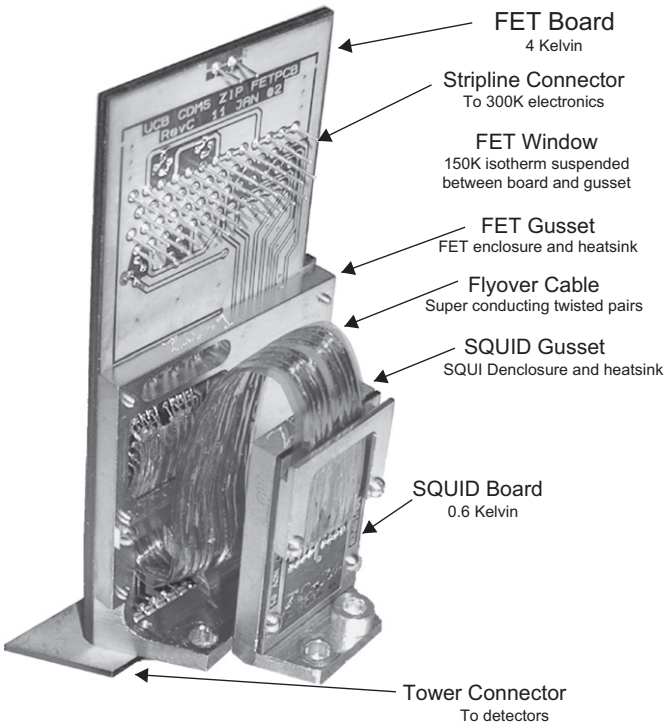

Fig. 2. Photograph of a SQuET card used in the CDMS II readout. The SQuET card is the name of the hybrid electronics card composed of a SQUID card (smaller, on the right) and a FET card (larger, on the back left side of the image) connected by the flyover.

2.5.1. FET card

2.5.1.1. CDMS I: BLIP FET card. The primary role of the FET card is to hold the FETs needed to read out the ionization signal and the BLIP phonon signal. This card also serves as the electrical path from the stripline down to other connections and components on the detector and detector holder, such as bias resistors, coupling capacitors, and LEDs. Also, in the ZIP design, the FET card interfaces with the SQUID card, used to read out the TESs.

The FET card is a printed circuit board made of multi-layered KAPTON of total thickness 1.5 mm. The electrical connections on the surface of the card are made of 1-ounce copper patterned using standard techniques. The card is mounted on the top of the 4 K stage of the Tower using a copper bracket (referred to as the "gusset") that provides a thermal connection to the bath as well as shielding the rest of the cryogenic electronics from the infra-red radiation emitted by the FETs. The upper section of the FET card has a 50 pin array of MILLMAX connectors that mates with a connector paddle on the stripline, which leads the

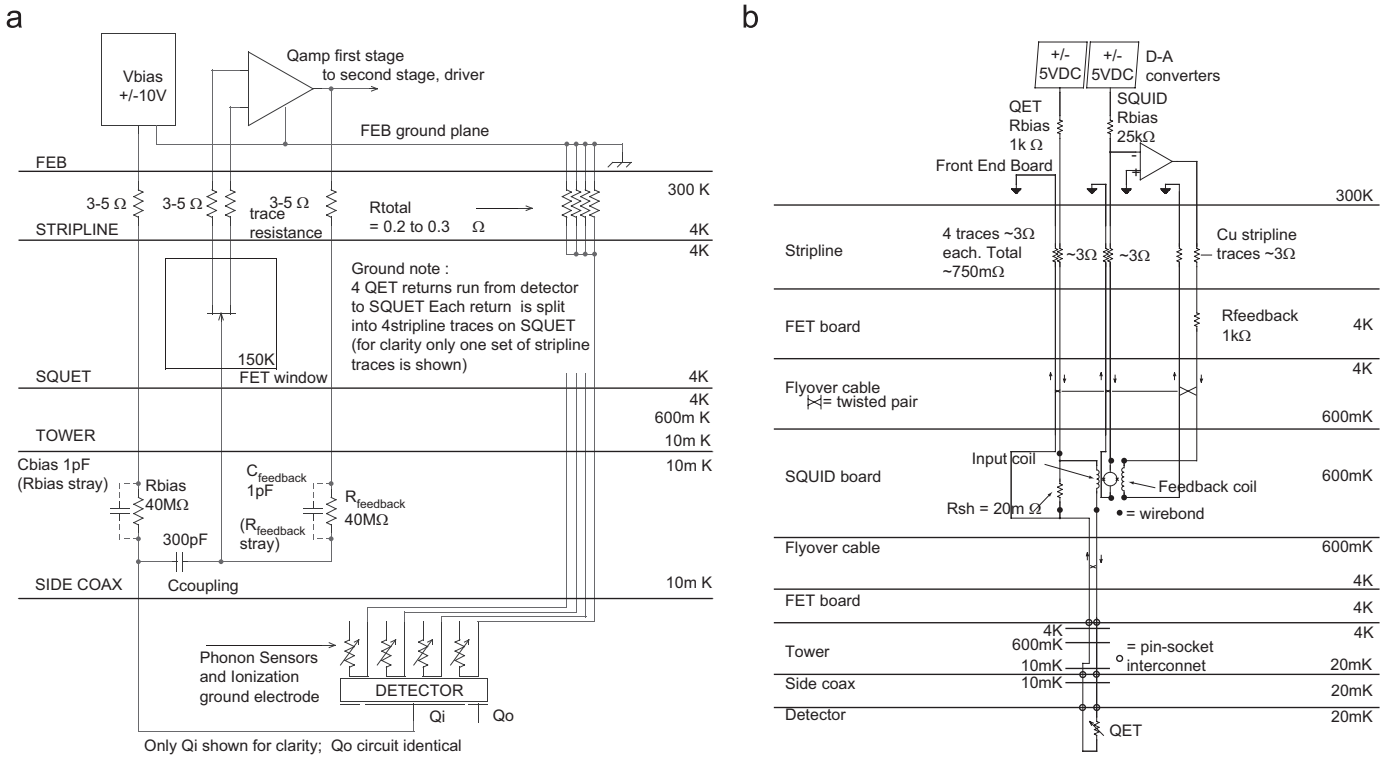

Fig. 3. Schematic diagram showing the thermal stages of the various components of: (a) the ionization and (b) phonon readout circuits.

signals to the "warm" electronics at room temperature (Fig. 2). The bottom edge of the card has a 16 pin array that mates with the Tower face leading down to a detector. The central part of the FET card is different in the BLIP and ZIP versions of the design.

In the BLIP design, the central part of the FET card contains a cavity where the FETs are operated. The cavity is coated with an infrared absorber [20] to absorb the thermal radiation from FETs. The front-end FET of the amplifier chain must operate at a temperature well above the 4 K stage of the refrigerator and dissipate several milliwatts (in our case 7 mW) of heat. A standard method is to mount the FET on a thin post with the heat sink attached to the 4 K stage such that the dissipated power brings the operating temperature into the correct range. Owing to the high channel count and associated space constraints, this layout is impractical for our needs. Applying the same principles, we designed and implemented a printed circuit board version of this concept. The four FETs needed to read out one detector are mounted in the center of a 0.15 mm-thick KAPTON window of dimensions 27.7 mm × 33.8 mm.

The vertical edges of the window are cut away so that the weak thermal coupling between the center of the window and the edges, which are at 4 K, allows the total power of 28 mW for the BLIP readout to heat the center to 150 K. Because the FETs are not turned on until the system is already cold, a startup heater (a 1 kΩ resistor) as well as a diode thermometer are included in the center of the window.

To obtain a sufficiently large thermal impedance in the window, the FETs, heater and the thermometer are connected to the copper circuit board on the surface of the card via sputtered platinum traces of approximately 3 μm thickness on the KAPTON window. For an area-to-length ratio A/l approximately equal to 0.5 μm, the platinum traces result in a resistance of about 1 Ω when cold and a thermal conductance that is negligible compared to the KAPTON.

We verified that this design yields optimal noise performance of the FET. In particular, we measured the noise of a FET mounted on a FET card window as a function of temperature (see Fig. 4). Indeed, the FETs self-heat to a near-optimal temperature of 150 K, where the noise is close to its minimum. Because of the difficulty of soldering components in the middle of the window, surface mount FETs, heater resistor and diode thermometers are connected to copper pads in the KAPTON window using silver-filled epoxy. The connection to the rigid section of the card is completed by the platinum traces which overlap the copper pads in the center and copper traces on the edges.

2.5.1.2. CDMS II: ZIP FET card. The FET card was revised for the CDMS II ZIP detectors, and the SQUID board and flyover were added. Fig. 2 shows a photograph and drawing of the resulting ZIP "SQUET" assembly with the main features identified. Due to resource constraints some compromises were made in the design in the changeover from BLIP to ZIP detectors. Although it might

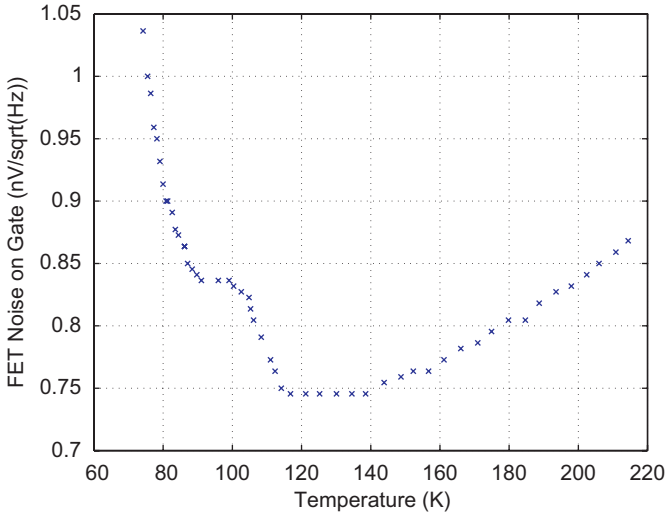

Fig. 4. JFET noise as a function of temperature. The noise measurements were taken at 10 kHz. At 120–140 K, the JFET noise is lowest ($\approx 0.75\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$). At 50 kHz, the trough reaches $0.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The design of the FET card window allows the FETs to self-heat at 150 K.

have been preferable to mount the SQUIDs between the FET card and detectors on the 600 mK stage of the tower wiring, that was not possible due to the constraints of the already existing towers. The new ZIP SQUET design went through several iterations before reaching the current version used in the CDMS II experiment.

The width of the FET window was reduced by half since only two FETs are required for the ZIP detector. To reduce the thermal load on the 4 K stage the FET bias power was reduced from 9 to 5 mW each. The window thermal impedance was increased to maintain the 150 K self-heating temperature. Several changes were made to increase reliability and ease of manufacture. The CDMS I window had been fabricated as part of the main FET card. The window had been fabricated over a cavity in the board in order to provide thermal isolation, but windows often sagged due to gas trapped under them during processing. To avoid this the CDMS II FET window was fabricated separately and glued onto the main board after the components were installed. The 3 μm platinum traces used in CDMS I had been difficult to deposit and had exhibited issues with cracking which caused noisy and intermittent connections. Those were replaced with 1 μm sputtered copper traces, employing the same material used for the stripline shield layers. The conductive epoxy used to glue the components to the window in CDMS I was difficult to work with and could also be unreliable and cause noise, so components are soldered in place on the CDMS II version. Soldering to a 1 μm copper trace proved to be challenging. Copper this thin has a tendency to dissolve into the solder, so future versions of the window will employ pattern-plating techniques to increase thicknesses of the copper in the soldering areas.

The first version of the CDMS II FET board mounted the SQUIDs in the space next to the 150 K FET window. Due to the poor thermalization and proximity to the 150 K window the SQUIDs remained too close to their superconducting transition temperature of 9.3 K. For that reason, and to improve SQUID signal-to-noise, it was decided to add a separate SQUID card at 600 mK. To operate the SQUIDs at 600 mK without extensively modifying the existing tower design it was decided to add a SQUID "spool" to the tower. A hole in the 4 K tower floor provides access to the 600 mK floor below. The spool is bolted to 600 mK and extends slightly above the 4 K floor without touching it. This provides a convenient mount and thermal connection for the new SQUID boards.

The first prototype of the SQUID + FET ("SQUET") cards employed bare 0.03 mm niobium–titanium wires stretched across the gap between the cards to connect the SQUIDs while maximizing thermal isolation. This proved too fragile for mass production and was replaced with the "flyover" cable. The flyover is made of twisted pairs of niobium–titanium superconducting wires which are copper–nickel clad and insulated with Formvar. Eight pairs are sandwiched between two pieces of polyimide and the whole cable is pressure laminated using epoxy. The copper–nickel cladding provides a good material for soldering while maintaining low thermal conductivity.

It was necessary to add an internal circuit layer to the CDMS II FET card to accommodate the additional SQUID wires. Conventional through-plating techniques are used to connect to this internal layer. A special plasma etch step is required for the polyimide material to clean the holes before plating. The first CDMS II FET card was made twice as thick (3.2 mm) because of a concern that flexing of the board during stripline connection might cause failures. The first flyover was made with wires with a 0.03 mm diameter NbTi core. This version was implemented without twisted pairs and contained a single signal return wire for two SQUIDs. Several problems soon became apparent. First, the single ground return and lack of twisted pairs created both resistive and inductive crosstalk between the two SQUIDs. Secondly, the small wire size resulted in a critical current which could be exceeded by the biasing electronics, driving the wires normal. Finally, once the wires were normal, the low thermal conductivity of the cable prevented the center portion of the cable length from returning to a superconducting state for several hours. The increased thickness of the polyimide FET board also resulted in poor thermalization of the flyover wires and failure of through-plated holes connecting internal layer circuitry.

The FET card was revised to improve thermalization by decreasing the thickness of the polyimide again and adding multiple through-plated holes to connect internal layer copper planes to the external layer planes and so to the FET card "gusset" at 4 K. A gap in the internal layer copper planes between the FET window and flyover sides of the FET card also provided increased thermal isolation

between them. Internal layer connections have been reliable through repeated thermal cycling from room temperature to 4 K and back. The present version of the flyover is made with wires with a 0.13 mm diameter NbTi core, clad to a 0.20 mm diameter with CuNi, and insulated with Formvar to an overall diameter of 0.23 mm. The intrinsic isolation of the SQUID array and coil circuits allow signals to be twisted with their corresponding returns and the returns are kept isolated all the way to the room temperature electronics. The twisted pairing, isolated returns and larger size of these wires resolved the crosstalk and critical current issues experienced with the first version.

2.5.2. SQUID card

The SQUID card holds the four SQUID arrays used to read out the transition edge sensors. This card is made of 0.813 mm thick polyimide with 1-ounce copper circuit boards on each side. Two flyovers are soldered to solder coated traces on the board which lead to bare copper wire bond pads. Two magnetic shields made of 0.0508 mm thick pieces of niobium foil are glued to the board polyimide without touching any copper to avoid eddy currents. These foil shields "pin" any ambient fields when the pass through their superconducting transition which prevents changing fields that could induce signals in the SQUIDs. An external 300 K μ metal shield reduces the ambient fields before the foil shields transition. Two SQUID array chips are glued to each piece of foil with a single drop of high peel-strength flexible epoxy to avoid thermal contraction induced stresses. Connections from gold pads on the chips to the copper pads on the board are made with 0.02 mm aluminum bond wire. A copper "gusset" protects the SQUIDs and bond wires and thermalizes the board to 600 mK. Strain relief clamps on each end of the flyover constrain the flyover wires at the solder joints to prevent breakage due to work hardening.

2.5.3. SQUIDs

The SQUID amplifiers used by CDMS are produced by the University of Colorado Denver and NIST (Boulder, Colorado) [21]. Each SQUID amplifier is actually formed from a series-array of 100 SQUIDS which operationally acts as a single SQUID but with a higher signal-to-noise ratio and better impedance matching with the downstream portion of the readout circuit. The SQUID arrays are characterized by:

- *Turns ratio*: Ratio of the number of turns in the input coil to the number of turns in the feedback coil (see Fig. 10 for an explanation of input/feedback coils). This determines the gain when operated in closed-loop mode and has a value of 10 for our devices.
- *Current-per-Φ_0*: Current in input or feedback coil corresponding to one quantum of magnetic flux Φ_0 in the SQUID. The value for our devices is 25 $\mu A/\Phi_0$ in the input coil and 250 $\mu A/\Phi_0$ in the feedback coil.
- *Self-inductance of the input coil*: $L = 0.25\,\mu H$.
- *V–Φ curve*: variation of the voltage across the SQUID with the change of flux Φ through the SQUID. The maximum peak-to-peak amplitude of the V–Φ curve (also called modulation depth) is typically 5 mV.

2.5.4. Responsivity

Responsivity $r = dV/dI$ is defined as the change in voltage V across the SQUID for a given change in current (either in the input or feedback coil). Equivalently, it is given by the slope of the V–Φ curve. For the SQUIDs, responsivity of 500–1000 Ω referred to input (RTI) is easily achievable.

The responsivity is important for two reasons. First, the input noise of the amplifier is amplified by the factor R_F/r, where $R_F = 1000\,\Omega$ is the feedback resistance. Hence, large responsivity reduces the impact of the amplifier noise and increases the signal-to-noise ratio. Second, the open-loop gain of the amplifier (which includes the overall responsivity as one of the gain factors) sets the bandwidth of the amplifier chain in the closed-loop mode. The amplifier is designed to give about 2 MHz bandwidth for $r = 1000\,\Omega$ RTI, but this value varies for different values of responsivity.

2.5.5. Resonance

Another issue of importance are the resonances of the SQUIDs. The resonances appear as distortions of the V–Φ curve and they tend to increase the SQUID noise significantly, so it is desirable to avoid them. The SQUID resonances are well known and have been studied in Ref. [22].

There are two types of resonances that appear in the SQUIDs used by the CDMS experiment. First, there is a "feedback" type resonance. In this case, the current through the tunnel junctions capacitively couples to the coils, which then feeds back inductively into the SQUID. On one slope of the V–Φ curve, the two effects will cancel each other out. On the other slope, however, the feedback will be positive and a resonance will be created. Note that this kind of resonance can appear only on one slope of the V–Φ curve.

Second, there is a "junction" type resonance. In this case, the bias of the SQUID introduces a voltage drop across the SQUID, which is, in turn, related to the frequency of the currents flowing through the SQUID loops. Changing the SQUID bias changes this frequency. If the frequency matches the natural frequency of the system, a resonance appears. Hence, this kind of resonance appears only at a particular, usually relatively large, SQUID bias voltage.

Both types of resonances can be avoided by applying relatively low SQUID bias and by locking the SQUID on the side of the V–Φ which has no feedback-type resonances.

2.5.6. Dynamic range

In the closed loop mode the system is locked at a single point on the V–Φ curve, or, equivalently, at a particular

value of current in the input coil. In practice, however, the amplifier is not infinitely fast, so the error signal, defined as the difference of a signal I_i in the input coil and the amplifier response I_r (as seen in the input coil), $e_i = I_i - I_r$, is non-zero. In particular, if the error signal during a phonon pulse is too large, it could cause loss of lock and the SQUID would jump one or multiple-integer number of cycles of the V–Φ curve. This, in turn, would distort the current pulse and affect the calorimetric measurement.

For the circuit shown in Fig. 10, the error signal is given by

$$e_i = \frac{I_i}{1 + (G_{OL}/10^4\,\Omega)} \tag{1}$$

where G_{OL} is the frequency-dependent open-loop gain of the amplifier (including the responsivity RTI) and it is given by

$$G_{OL} = \frac{6000r}{\sqrt{1 + \left(\frac{f}{2.4\,\mathrm{kHz}}\right)^2}}. \tag{2}$$

For example, for responsivity $r = 1000\,\Omega$ RTI and at 100 kHz (which is higher than the relevant frequency range for the signal), the error signal amounts only to about 6% of the input signal. Given that the typical phonon signal has amplitude of 1–10 μA, the error signal is not expected to exceed 1 μA, which has been experimentally verified. Furthermore, since the input coil current corresponding to Φ_0 (or, equivalently, to one V–Φ cycle) is about 25 μA, it is clear that the error signal is sufficiently small to keep the feedback stable.

2.6. Stripline

The transmission of the signals from the FET card to room temperature is accomplished with a multi-layer shielded flex circuit approximately 2.5 cm wide and 300 cm long made of copper and KAPTON. Because of high channel count and the 50 traces per circuit, we chose a printed circuit solution. A large stack of flex circuits can be effectively heat sunk through a set of copper pressplates and copper shims. The strip line fabrication was more difficult than anticipated due to the low production yield of such a long circuit.

The stripline's signal layer is made up of fifty 0.018 mm-thick (1/2-ounce) copper traces on 0.381 mm centers. It is sandwiched between two 0.127 mm-thick KAPTON layers, two sputtered copper ground planes, and two 0.0254 mm-thick KAPTON insulating coverlays. The cold end is terminated with a stiffener card that holds an array of pins that mate with the FET card and the warm end is soldered to a standard 50-pin D-subminiature connector. When deployed in the main experiment's cryostat [14], the striplines are heatsunk at both LHe and LN temperatures with approximately 15 cm between room temperature and LN and 100 cm between LN and LHe. These lengths are a compromise between thermal loading and increased resistance. In particular, we can only tolerate an impedance of 1–2 Ω on the source line of the FET.

To date, we have deployed stacks of up to 30 strip lines in the SUF cryostat. To minimize infrared leakage into the cryostat, due to the transparency of KAPTON in the IR band, the strip lines are suspended in a set of copper baffles in the electronics entry tube, or "E-stem." Each baffle is painted with an IR-absorbing epoxy mixture and has weak thermal coupling to the striplines so that the thermal gradient can be maintained [20].

3. Ionization signal readout

In this section we describe the principles and noise performance of the ionization signal readout system. A more detailed description of this system is given in Ref. [23].

The circuit used to read out the ionization signal can be simplified as shown in Fig. 5. A voltage bias (typically around 3 V) is used to separate the electron–hole pairs that are created in the Ge (Si) crystal when an interaction takes place. This charge Q creates a voltage across the coupling capacitor C_c (and at the gate of the JFET). The amplifier reacts by charging the feedback capacitor C_F to bring the voltage level at the gate to zero. The feedback capacitor is subsequently discharged through the feedback resistor R_F. The voltage ionization signal is, therefore, created at the feedback capacitor and its amplitude (to zeroth order) is $V = Q/C_F$. The decay time of the ionization pulses is set by the $R_F C_F$ circuit and it is typically 40 μs. The rise-time of the ionization pulses is determined by the details of the amplifier and it is typically around 1 μs. The noise at the input of the amplifier (that is, at the gate of the FET) is amplified by the ratio of the total gate-to-ground capacitance to the feedback capacitance C_F. The total gate-to-ground capacitance is a combination of the detector capacitance (typically $C_D \approx 50$ pF), coupling capacitance ($C_c = 300$ pF), and the effective parasitic capacitance (measured $C_p \approx 100$ pF).

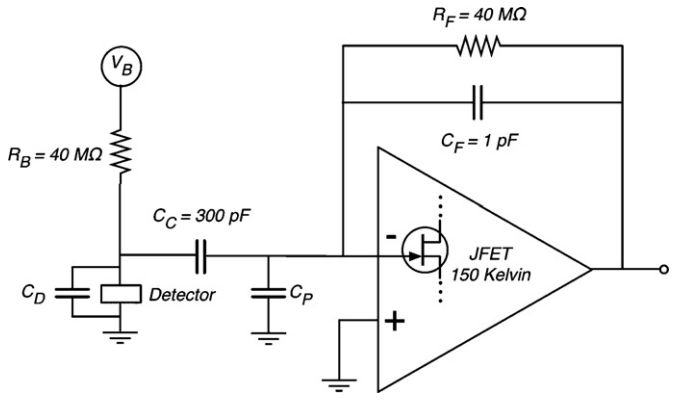

Fig. 5. Charge readout circuit. The heart of the amplifier is a JFET. The parasitic capacitance has been measured to be $C_p = 100$ pF and the detector capacitance is typically $C_D = 50$ pF. G denotes the gate of the JFET.

The heart of the amplifier is a JFET. The primary advantage of the JFET is its high input impedance, which allows good charge collection efficiency. Moreover, the JFET is characterized by low voltage noise performance. The total voltage noise of the circuit shown in Fig. 5 is given by the following expression [19]:

$$e_0^2 = |A(f)|^2 \left\{ e_{\mathrm{FET}}^2 \left((C_{\mathrm{D}} + C_{\mathrm{p}} + C_{\mathrm{F}})^2 (2\pi f)^2 + \left(\frac{1}{R_{\mathrm{F}}} + \frac{1}{R_{\mathrm{b}}} \right)^2 \right) + 4kT \left(\frac{1}{R_{\mathrm{F}}} + \frac{1}{R_{\mathrm{b}}} \right) \right\} \quad (3)$$

where

$$A(f) = \frac{R_{\mathrm{f}}}{1 + 2\pi i f R_{\mathrm{F}} C_{\mathrm{F}}}. \quad (4)$$

k is the Boltzmann constant, $T = 20\,\mathrm{mK}$ is the temperature of the bias and feedback resistors, and e_{FET} is the voltage noise of the JFET (it is typically $0.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 50 kHz, as discussed in Section 2). Eq. (3) predicts that at frequencies above roughly 1 kHz the JFET noise dominates the total output noise of the system. Furthermore, at these frequencies the noise spectrum should be flat at $\approx 100\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, which has been experimentally confirmed (see Fig. 6). The bandwidth of the system is set by the amplifier; the $-3\,\mathrm{dB}$ point is at $\approx 160\,\mathrm{kHz}$.

To estimate the lowest signal observable by this readout system, one can integrate the power spectral density to obtain the variance of noise of $\sigma^2 \approx 2 \times 10^{-9}\,\mathrm{V}^2$. Define the lowest observable signal to have amplitude of $2\sigma \approx 0.1\,\mathrm{mV}$, corresponding to 0.1 fC of charge on the feedback capacitor. Since 3.8 eV is needed to create an electron-hole pair in Si (3 eV in Ge), the lowest energy that can be observed by the ionization channel on a Si detector is $\approx$ 2.5 keV ($\approx$ 2 keV for a Ge detector).

4. NTD thermal phonon signal readout

The phonon signal in the BLIP detectors was read out using the NTD Ge thermistors [7,8,24]. NTD germanium is made by exposing Ge to neutrons in a nuclear reactor. The nuclear reactions create Ga impurities out of Ge atoms, so the material is strongly p-type. Neutrons have sufficiently long mean-free-paths that the material is uniformly doped even on the few mm scale. The density of impurities is sufficiently large that the electrons can hop between impurity sites, making the material conduct (typically operated at 1–2 MΩ). The thermistors are eutectically bonded to the surface of the Ge crystals. The eutectic bonding provides a reliable and reproducible interface that is transparent to the low energy phonons [25]. Two NTD thermistors are bonded on each detector. This allows us to discriminate against thermal fluctuations in a single thermistor.

The basic principle behind this readout system is described as follows: an event in the crystal deposits a δ-function of energy in the phonon system of the crystal. The phonon system heats up, and it warms up the electron system via the electron–phonon coupling, yielding a measurable change in resistance of the thermistor. The couplings are chosen so that the electron system senses the phonon system temperature before it relaxes back to the temperature of the bath.

The readout system is schematically shown in Fig. 7. Since $\mathrm{d}R/\mathrm{d}T < 0$, it is necessary to current-bias the thermistor (to avoid thermal run-away), which is achieved using the voltage bias V_{b} and the bias resistor R_{b}. The rise and fall times of the BLIP phonon signal are 5 and 50 ms, respectively, corresponding to poles at 3 and 30 Hz. However, as shown in Fig. 8, below 500 Hz, the $1/f$ noise (from the JFET, thermistor and electrical connections) and 60 Hz noise (from the power supplies) become significant. For this reason, it is advantageous to use a lock-in technique. We replace the DC bias with a 1 kHz sine-wave bias, as the noise environment at 1 kHz is very clean (see Fig. 8). Although the power dissipation in the thermistor oscillates at 1 kHz, the electron and phonon temperatures cannot respond as quickly and the system behaves as it would to a constant input power.

The slow pulse signal is "mixed" with the 1 kHz bias in the thermistor, and appears around 1 kHz, far from the low-frequency noise. The signal is square wave demodulated

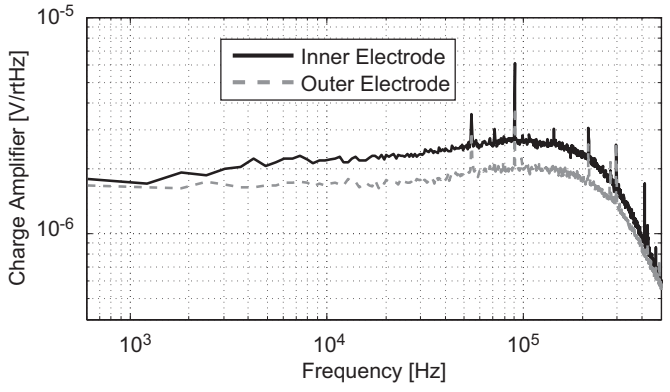

Fig. 6. Typical noise spectra obtained while operating ZIP detectors. Two charge channels on the same detectors are shown, corresponding to the inner and outer charge electrodes.

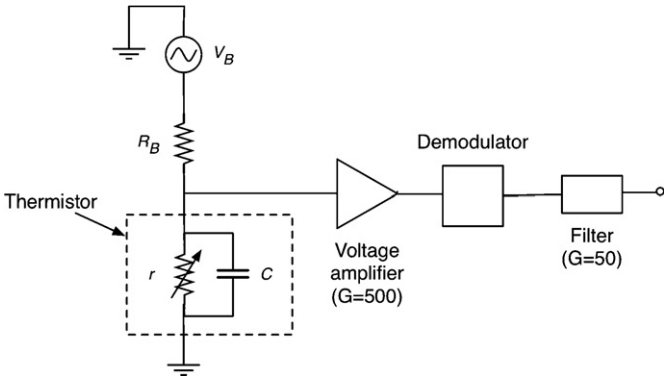

Fig. 7. The readout system schematic for the BLIP phonon channels.

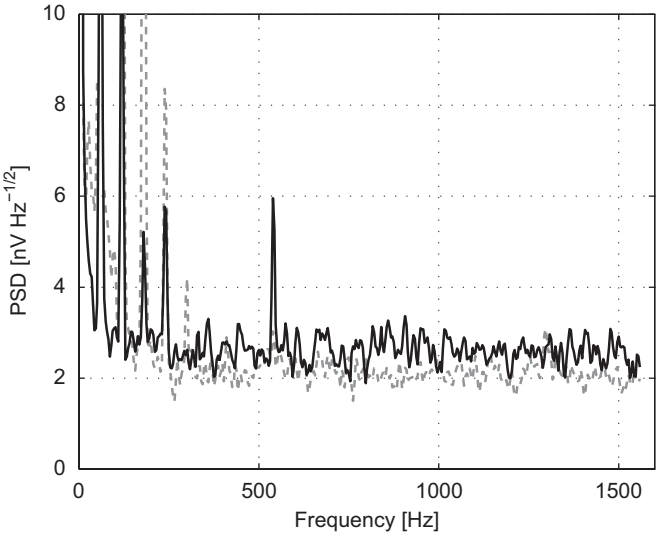

Fig. 8. The noise spectrum of the BLIP phonon channels. dashed: Phonon sensor 1. Solid: Phonon sensor 2.

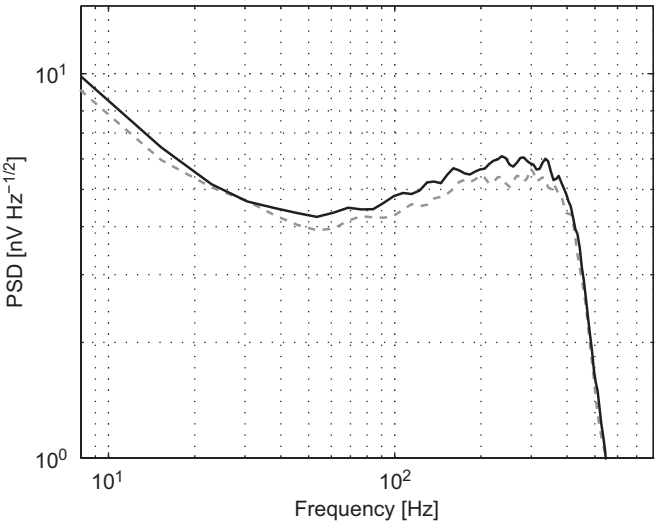

Fig. 9. The noise spectra of the BLIP phonon channels as measured with the lock-in amplifier. dashed: Phonon sensor 1. Solid: phonon sensor 2.

using the zero crossings of the signal itself. Prior to demodulation, the signal is low-pass filtered with a 2-pole 1.85-kHz-cutoff filter to prevent the square wave demodulation from mixing the higher frequency noise into the region of interest. The demodulated signal is again low-pass filtered, this time with a 8-pole 450 Hz-cutoff Butterworth filter, to remove the frequency components near 2, 4 kHz etc. Fig. 9 shows the noise spectrum as measured with the lock-in amplifier.

Integrating this spectrum gives the noise variance of about $1.3 \times 10^{-14}\,\mathrm{V}^2$. Empirically, 1 keV of energy corresponds to approximately 160 nV in pulse height, therefore the baseline resolution is about 700 eV, which was confirmed experimentally. For further details regarding the BLIP phonon readout system, see [15]. Further details on the performance of the detectors and the readout system can be found in Refs. [5,6,15].

5. QET athermal phonon signal readout

5.1. Principles of operation

The CDMS II experiment uses the QET sensors to measure the athermal phonon signal. The readout system for our implementation, which is a low-impedance voltage-biased TES, is based on SQUIDs. The low-noise characteristics of the SQUIDs make them suitable for amplification of very small signals. The readout system used for the phonon signal is consequently quite different from the one used for the ionization signal. The simplified schematic is shown in Fig. 10.

As mentioned above, the phonon signal is measured using tungsten TESs. Briefly, the phonons generated by an event in the crystal cause an increase in the temperature of the sensor, which is operated at the superconducting transition edge, therefore increasing its resistance (denoted by R_s in Fig. 10). Since the typical operating value of R_s is 100 mΩ, the shunt resistor $R_{sh} = 20\,\mathrm{m\Omega}$ keeps the sensor voltage biased. It follows then, that a change in R_s causes a change in the current flowing through the input coil of the SQUID, which in turn changes the voltage across the SQUID (that is, at the input of the amplifier on Fig. 10). Furthermore, with the amplifier operated in closed-loop mode, negative feedback acts to null the flux through the SQUID. In addition to providing a good impedance matching to the cryogenic and room temperature amplifier stages, the SQUIDs provide a current gain of 10 due to the relative mutual inductances of the input and feedback coils.

A phonon-mediated pulse is characterized by a rise-time of typically 10 μs and fall-time of typically 200 μs. However, these characteristic times strongly depend on the type of detector and the event itself, as well as on the charge bias voltage which affects the energy of phonons produced by charge carriers drifting through the potential. (Phonons thus produced are referred to as NTL phonons [26,27].)

5.2. Noise

There are several contributions to the total output noise of the phonon channels. We separately consider the SQUID noise as being particularly interesting to this discussion.

5.2.1. SQUID noise

The noise of the SQUID comes from the Johnson noise of the shunt resistors used to dampen the resonant behavior. Since the SQUIDs are operated at 600 mK, it is expected that they will have low-noise performance.

The noise of the SQUID can be thought of in terms of the flux noise passing through it or, equivalently, as the current noise in the input coil. In order to measure this noise, we set $R_s = \infty$ (that is, we open the circuit on the

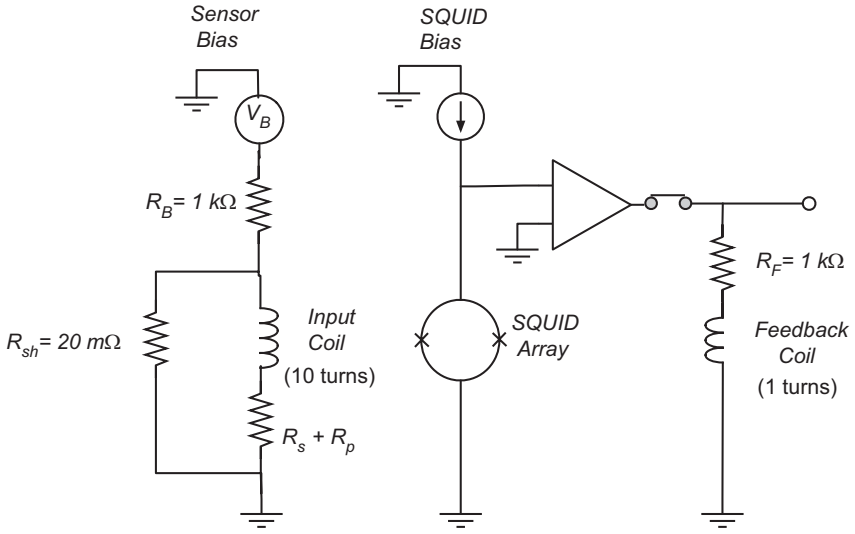

Fig. 10. The phonon channel readout system. The system is in the open-loop mode if the switch is open and in the closed-loop mode if the switch is closed.

input side of Fig. 10). The total output noise, then, has only two contributions: the SQUID noise itself and the input amplifier noise. The input amplifier noise is amplified by a gain of R_F/r referred to feedback (RTFb), whereas the SQUID noise is amplified by the turns ratio and the R_F resistor. Hence, by measuring the total output noise at different values of responsivity, we can separate the two noise contributions.

We changed the value of responsivity by locking the SQUID at different points on the V–Φ curve. Points were taken on both the stable slope and the slope that is unstable due to feedback-type resonances. At each point, we measured the noise in the flat region of the spectrum, around 5–10 kHz. The results are shown in the Fig. 11, where the crosses correspond to the measurements taken on the stable slope and the open circles to the unstable slope. We observed that the noise on the unstable slope is larger than on the stable slope. Some points taken on the stable slope exhibit a higher than expected noise, however, this is attributable to the SQUIDs being locked very close to the junction type resonance during those measurements.

Keeping only the points far from the junction resonances on the stable slope of the V–Φ curve results in a least-square fit for the SQUID noise of $1\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ RTI and input-amplifier noise of $1.2\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (consistent with the amplifier noise measurement on the bench). It is important to note that the responsivity has a strong impact on the contribution of the amplifier noise. In particular, r as low as 100 Ω RTFb (or 1000 Ω RTI) can make the amplifier noise contribution comparable to the SQUID noise contribution.

5.2.2. Johnson noise

The total Johnson noise of the phonon channel has several contributions. As shown in Fig. 10, the resistances R_s, R_{sh}, and R_p all contribute Johnson noise; the SQUID and amplifier must also be taken into account. The total

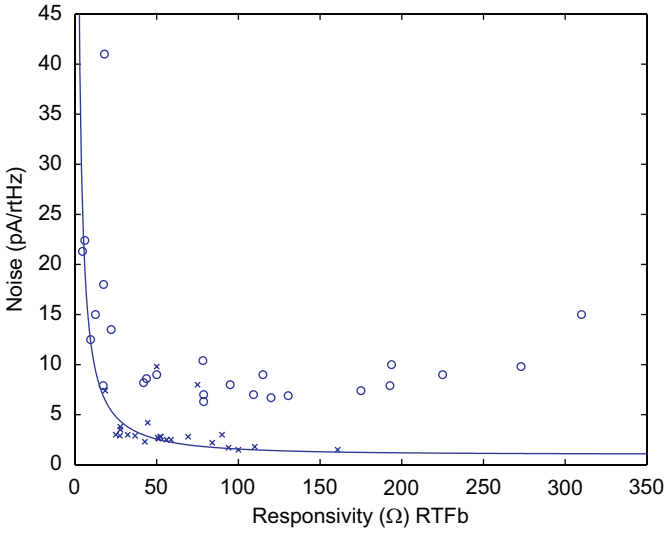

Fig. 11. Noise vs responsivity plot. The crosses (×) refer to the stable slope of the V–Φ curve and the open circles (○) refer the unstable slope (with respect to feedback-type resonances).

current noise in the input coil is given by [28]

$$i_n^2 = 4k\frac{R_s T_s + R_{sh} T_{sh} + R_p T_p}{(R_s + R_p + R_{sh})^2} + i_{SQUID}^2. \quad (5)$$

Here, $T_s = 65\,\mathrm{mK}$, $T_{sh} = 600\,\mathrm{mK}$ and T_p are the temperatures of the sensor, shunt and parasitic resistances respectively and k is the Boltzmann constant. It should be noted that Eq. (5) is valid in the quiescent state, i.e. where there is no pulse occurring and the sensor resistance is constant. Taking the effects of ETF into consideration the power spectral density of the current noise is given:

$$i_\omega^2 = i_n^2\left[\frac{\left(\frac{n^2}{\alpha^2} + \omega^2\tau_{eff}^2\right)}{1+\omega^2\tau_{eff}^2} + \frac{\frac{n}{2}}{1+\omega^2\tau_{eff}^2}\right] \quad (6)$$

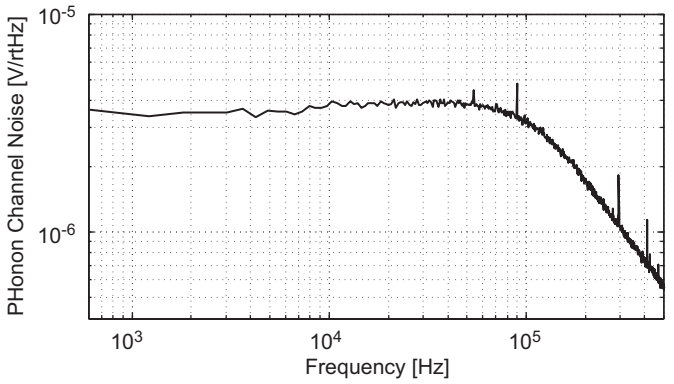

Fig. 12. Total noise in the phonon channel observed in the usual TES operating mode.

where α, n, and τ_{eff} are parameters which describe the electro-thermal feedback aspect of the TES, and are fully explained in Ref. [28]. For the ZIP and Tower design we have parasitic resistances of about 1 mΩ from the MILLMAX connector pins both at the base temperature stage, and more importantly, at about 4 K where the side-coax mates with the FET card.

The total output voltage noise is given by

$$v_{\mathrm{n}} = \sqrt{i_{\mathrm{n}}^2 (10R_{\mathrm{F}})^2 + v_{\mathrm{e}}^2 \left(\frac{R_{\mathrm{F}}}{r}\right)^2} \tag{7}$$

where v_{e} is the input voltage noise of the amplifier. The typical total parasitic resistance R_{p} is 6–8 mΩ and the typical shunt resistance R_{sh} is 20 mΩ. At the usual TES operating point the resistance R_{s} is 100–200 mΩ. This value of the sensor resistance is chosen to maximize the signal-to-noise ratio and is set by the TES bias point. Furthermore, the shunt resistance is the dominant voltage noise source, although R_{s} strongly affects the total current noise in the input coil. For $r = 1000\,\Omega$ RTI Eqs. (5) and (7) give a total output noise of $10\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ RTI in the flat region of the spectrum. This has been experimentally confirmed, as shown in Fig. 12.

5.3. Bandwidth

When discussing the bandwidth, it is useful to separate two of the noise components. The current noise in the input coil of the SQUID is rolled off by the L/R filter on the input side of the SQUID. Here $L = 0.25\,\mu\mathrm{H}$ is the self-inductance of the input coil and R is the combined resistance on the input side, dominated by R_{s} in the usual mode of operation (as discussed above, optimization of the signal-to-noise ratio leads to sensor resistance R_{s} in the range 100–200 mΩ). Therefore, the current noise in the input coil is frequency dependent in the output and it has a −3 dB point at 65–130 kHz, (other steps in the electronics chain may make this roll-off faster). The second noise component is frequency independent in the output and it is composed of the amplifier noise and the digitizer noise. It contributes $5\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ or less, depending on the digitization rate. Hence, the total output noise is dominated by the amplifier and digitizer noise components at frequencies much above 130 kHz. However, at these frequencies, the signal-to-noise ratio is typically already less than one for most phonon pulses. This is confirmed by the data shown in Fig. 12.

Note also that the roll-off described above is dynamic. In other words, during an interaction R_{s} first increases (since the sensor is kept at its superconducting transition edge) and then falls back to its original value. Hence, the −3 dB point of the L/R filter first increases during a phonon pulse and then falls back to its original value. Furthermore, the amplifier response is not totally frequency independent. Its response depends on the responsivity and for reasonable $r = 1000\,\Omega$ RTI, the −3 dB point of the amplifier is at 2.1 MHz. This is far above the frequency range of the signal, so the frequency dependence of the amplifier can be neglected.

As in the case of the ionization channels, one can attempt to estimate the lowest energy observable by the phonon readout system. Integration of the power spectral density gives the noise variance σ^2 of about $10^{-17}\,\mathrm{A}^2$. Hence, signals are observable down to, say, the 2σ point of 6 nA. For a typical voltage bias of 5 μV, this corresponds to a signal power of 30 fW. Alternatively, for a pulse with characteristic decay time of 300 μs, this corresponds to a collected energy of 60 eV for a 100% phonon collection efficiency. This energy is the lowest signal observable by the setup described above. Note, however, that this is not necessarily the lowest observable recoil energy of an event. The observed signal strongly depends on the value of the charge bias (which affects the energy carried by the NTL phonons) and on the phonon collection efficiency.

6. Conclusion and summary

In this paper we have described the detectors, cryogenic hardware and readout system used to process the signals obtained by the CDMS detectors. We have discussed the hardware constraints of deploying a large number of low-temperature detector in a low-background environment required for a rare-event search experiment. We have also reviewed the performance measurements of the readout system with respect to functionality, noise, and bandwidth. The BLIP version of the readout system, along with a preliminary version of the ZIP system, was used in 1998–1999 and led to the measurements reported in Refs. [6,5]. The final ZIP readout system was used to read out six detectors in a run at the Stanford Underground Facility during 2001–2002 as well as the detectors that have been installed and operated at the CDMS II site in the Soudan Mine Underground Laboratory since then.

Acknowledgments

Past and recent support for this work through the National Science Foundation came from the Center for

Particle Astrophysics, an NSF Science and Technology Center operated by the University of California, Berkeley, under Cooperative Agreement No. AST-91-20005, and from NSF Grant Nos. PHY-9722414, AST-9978911, PHY-0503729, PHY-0503629 and PHY-0504224 and through the Department of Energy under Contracts DE-AC03-76SF00098, DE-FG03-90ER40569, and DE-FG03-91ER40618.

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